1. Document Purpose and its Organization

Speech Recognition is an ideal means to give commands to machines. It would realize the dream that machines would operate as you wish when you, without any complicated key operations, simply asked to them in words as you did to friends. As one step to the dream, Toshiba has developed the speaker dependent isolated word recognition device set TC8861F/TC8862F/TMP80C50AU.

This document describes the recognition device set from the following view points. First, it overviews hardware and software about the recognition device set as a comprehensive introduction. Secondly, it thoroughly presents hardware details in order to give hardware engineers enough information to design application circuits. Then it roughly reviews host computer programs to control the recognition device set. However it limits those programs' explanations to only fundamental items and gives a role for detail description to another document "Speaker Dependent Speech Recognition Software Manual". Software engineers developing host system programs are strongly recommended to read the software manual.

The organization on this document is as follows: Chapter 2 deals with features on the recognition device set and chapter 3 and 4 describes hardware configuration and software functions respectively. Chapter 5 focuses on description about interface hardware used to control the recognition device set by host systems. Chapter 6 handles interface software aspect, along with data formats for host-device data communication. Chapter 7 presents an application circuitry example employing the devices. Chapter 8 explains function, pin assignment and pin description for each device. Chapter 9 deals with electrical characteristics and Chapter 10 depicts package dimensions.

2. Introduction

The speaker dependent isolated word recognition device set consists of TC8861F, TC8862F, TMP80C50AU* and 64 or 256kbit static RAMs. The device set contains the whole circuits and functions necessary to recognize voices, so it is easily employed in a wide range of applications. The device set operates with commands given by a host computer.

2.1 Features of Recognition Device Set

(1) Reference pattern generation** with Differential Filter Method***. Three utterances per word required.

(2) Pattern matching with Multiple Similarity method****.

(3) Configuration: TC8861F, TC8862F, TMP80C50AU and static RAMs.

(4) Recognition rate: 93.0%±1%
(Vocabulary: The 78 most frequent Japanese sir names
Test Speakers: 8 Japanese (males, females))

(5) Vocabulary numbers: Maximum 78 (when 256kbit SRAM employed)

(6) Response time: 0.3~0.5 seconds.
(Defined as the time length from the utterance end point to the time point of result return to the host computer.)

(7) Input voice time length allowed: 0.12~1.92 seconds.

(8) Reference pattern bank setting: Every reference pattern can be, if necessary, allocated into one of 8 banks so that the device set executes pattern matching with a particularly limited vocabularies in the designated bank.

(9) Rejection:
On registration: If three utterances for a word shows characteristic differences among them, the device set rejects these three utterances and then requires another three for the same word again.
On recognition: If a voice to be recognized presents low similarity to all the vocabularies registered, the device set rejects input voice and requests another input voice.

(10) Directly connectable to a voice input microphone.

(11) Power saving mode available:

(12) +5 single power supply: (Caution: The separate second power supply is recommended to be employed in order to improve the recognition rate.)

* TMP80C50AU operates with program codes embedded in an on-chip Mask ROM. The standard program codes for speaker dependent speech recognition are readily prepared on the on-chip Mask ROM of the part No.TMP80C50AU-9537UZ.

** Reference patterns must be readily generated on static RAMs through registration process requiring users to store vocabularies by their own voices. These patterns are examined to choose the most possible vocabulary candidate when voice to be recognized enters the device set.

*** The method uniquely developed by Toshiba.

**** The method jointly developed by the Agency of Industrial Science & Technology of MITI, and Toshiba. The device set adopts the Patent "Multiple Similarity Method" (Japanese Patent No.739890) under license of the Japanese Industrial Technology Association. Details are to be referred to references (1), (2).

References

(1) Y.Takebayashi, et al., "Telephone Speech Recognition Using a Hybrid Method", IEEE 7th International Conference on Pattern Recognition Proc., pp.1232-1235, 1984.

(2) H.Sekiguchi, et al., "A Three-Chip LSI System for Speaker Independent Isolated Word Recognition by Multiple Similarity Method", IEEE ICCE Dig. of Tech. Papers pp.240-241, 1987.

3. Hardware on Device Set

The purpose of this chapter is to outline the device set hardware. The device set configuration is mentioned in 3.1 and each device on the set is briefly described in 3.2 from the functional viewpoint.

3.1 Device Set Block Diagram

The recognition device set is comprised of minimum 4 chips. They are TC8861F analog processor, TC8862F digital processor, TMP80C50AU system controller and 64kbit or 256kbit C-MOS static RAMs.

Fig. 3.1 shows the hardware organization of the device set.

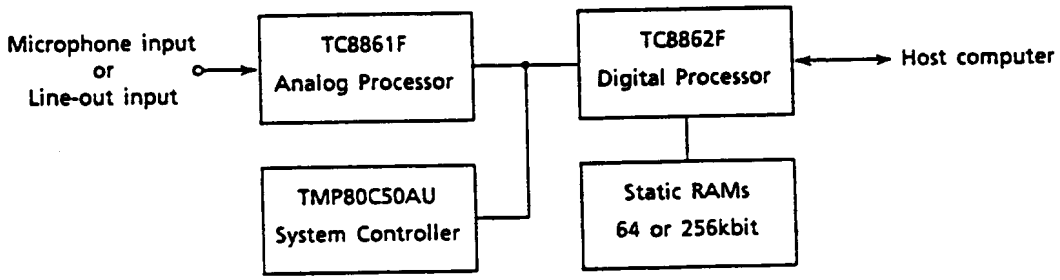


Fig. 3.1 Hardware Organization of Device Set

The static RAM capacity determines the number of vocabulary to be recognized. Table 3.1 shows static RAM connection versus vocabulary capacity.

Table 3.1 Relationship between static RAM capacity and recognition vocabulary number

Static RAM connected		Recognition Vocabulary Number
TC5565PL-15*	×1	Maximum 19 words
	×2	Maximum 38 words
	×3	Maximum 58 words
	×4	Maximum 78 words
TC55257PL-10	×1	Maximum 78 words

* Any other static RAM with access time 200ns and less is connectable.

3.2 Device Features

Features on each device are roughly described here. More details for each are mentioned in Chapter 8.

3.2.1 TC8861F Analog Processor

(1) Built-in 7 channel band-pass filters and analog-to-digital (A to D) converter with 10bit resolution for acoustic analysis of voice signals.

(2) System clock 2MHz (supplied by TC8862F).

(3) 60-pin Mini Flat Package.

3.2.2 TC8862F Digital Processor

(1) Built-in MS calculation hardware, external reference pattern memory I/F, host computer I/F and 8kbit scratch-pad RAM.

(2) System clock 4MHz (Built-in oscillation circuit for ceramic resonator).

(3) 100-pin Flat Package.

3.2.3 TMP80C50AU System Controller

(1) Micro controller unit performing command analysis, command execution and overall management of the device set.

(2) System clock 11MHz (Built-in oscillation circuit for ceramic resonator).

(3) 44-pin Micro Flat Package.

Fig. 3.2 illustrates the device set block diagram showing both sub-blocks in each device and signal connections among devices.

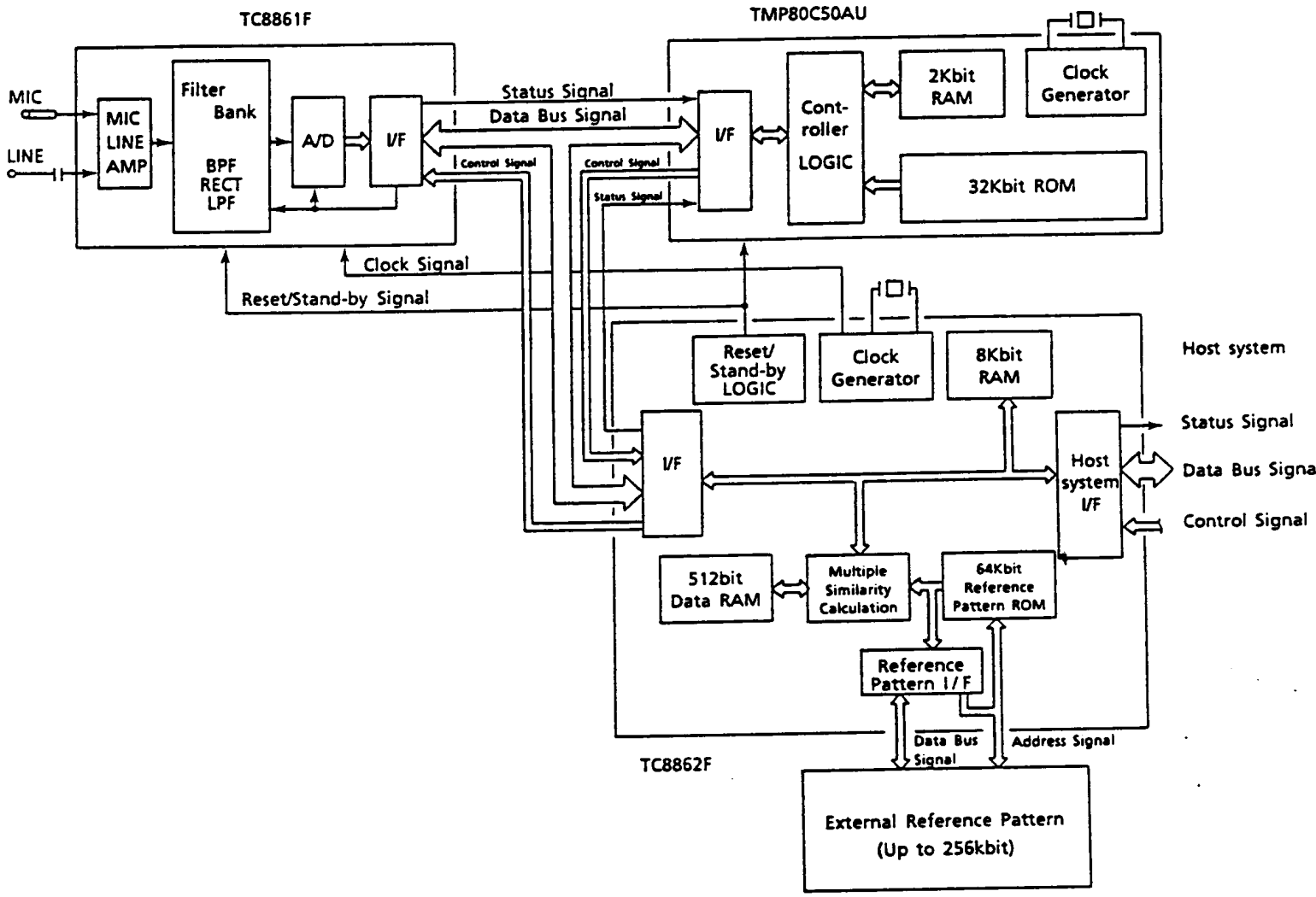


Fig. 3.2 Device Set Block Diagram

4. Device Set Functional Organization

The device set provides 9 functions as described in Fig. 4.1. They includes reference pattern initialization, reference pattern registration, reference pattern deletion, recognition, reference pattern bank setting, TC8861F filter offset compensation, system reset, system stand-by on and system stand-by off. These functions are embedded in 4 LSI hardware and software program on the TMP80C50AU on-chip Mask ROM. For user's convenience, Toshiba supplies a readily programmed Mask-ROM TMP80C50AU* for the functions. (The part No.TMP80C50AU-9537UZ)

All the functions are executed by commands given by a host computer. Therefore the device set always needs a host computer for its operations. Practical description about command operations are given in Chapter 5 and Chapter 6 in terms of both hardware aspects and software aspects, respectively.

The two most important functions among nine are reference pattern registration and recognition. 4.1 and 4.2 describe these two functions respectively. 4.3 shows the system state transfer chart to overview the device set functional organization.

* Toshiba holds the copy-right for the programs embedded in the Mask-ROM.

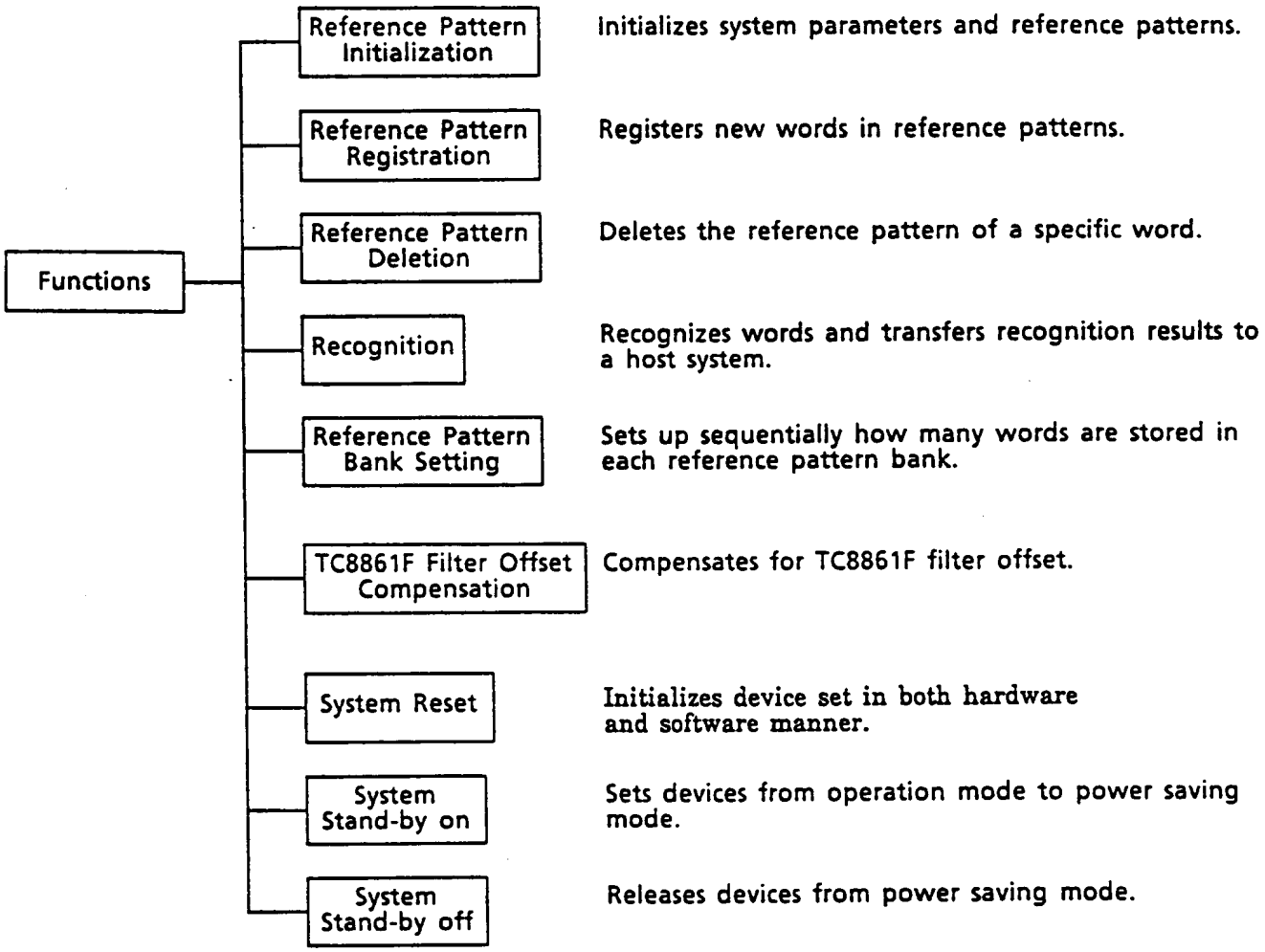


Fig. 4.1 Functional Organization of Device Set

4.1 Reference Pattern Registration

Reference patterns for vocabularies to be recognized are necessarily stored in external RAMs before recognition is executed. An action to store reference patterns is called registration. The registration produces a reference pattern for a word by analyzing three utterances required to give. The execution sequence for reference pattern production in the device set is itemized below and is illustrated in Fig. 4.2.

(1) TC8861F receives three utterances per word in order to perform both acoustic analysis on voice signals and A to D conversion on analyzed analog signals.

(2) TMP80C50AU detects word boundaries on A to D output signals. Then it operates arithmetic calculation to prepare a reference pattern. Digitized raw voice signal are stored in input voice RAM.

(3) The prepared reference pattern is, through both Multiple Similarity (MS) calculation block and reference pattern I/F, transferred to and is stored in external reference pattern static RAMs.

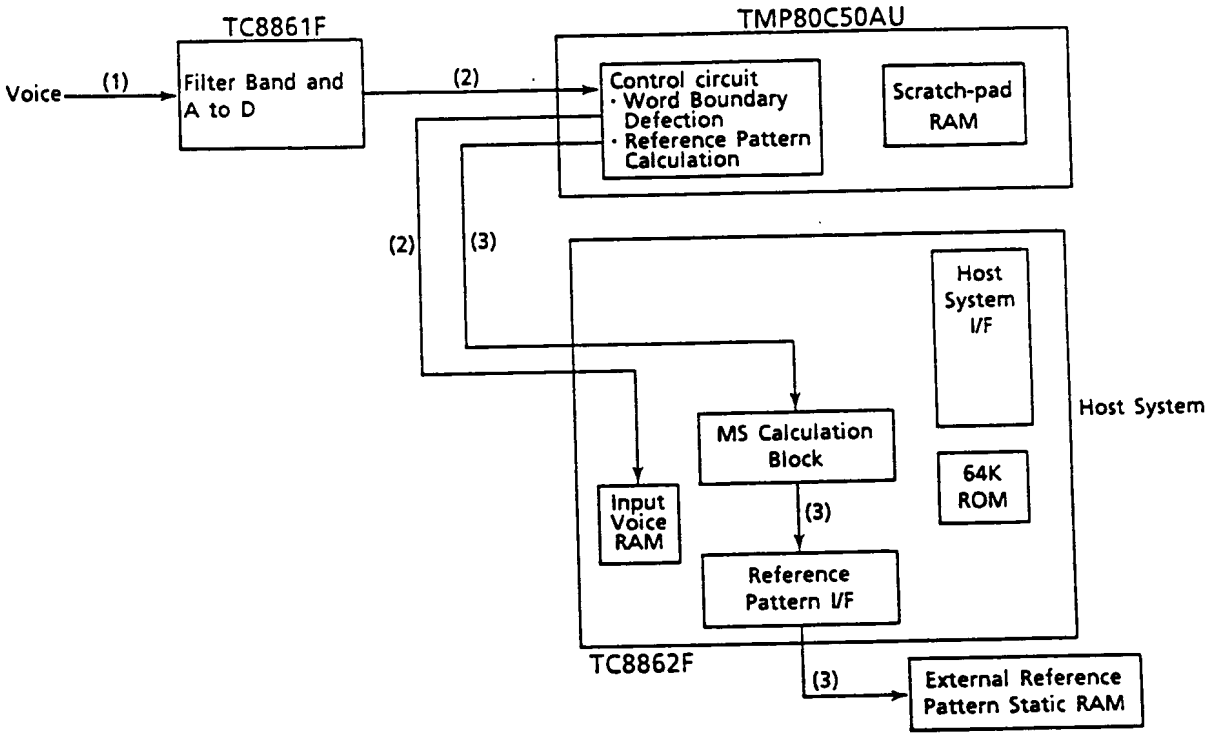


Fig. 4.2 Data Flow in Reference Pattern Registration

4.2 Recognition

The device set recognizes voices in a way that it compares input voice features with vocabulary reference patterns beforehand stored in external reference pattern static RAMs. The recognition results indicating most possible word candidates for input words are transferred to a host computer.

The functional process is itemized below and is charted in Fig. 4.3.

(1) TC8861F receives a voice to be recognize in order to perform both its acoustic analysis and A to D conversion on analyzed analog signals.

(2) TMP80C50AU detects word boundary on A to D output signals.
Then the detected signals are transmitted to an input voice RAM on TC8862F.

(3) TC8862F transfers the detected signals from the RAM to MS calculation block on TC8862F, where the similarity of the detected signals to all reference patterns stored in external RAMs is examined.

(4) All similarity scores calculated for the whole vocabularies are transferred to TMP80C50AU.

(5) The scores are saved in scratch-pad memory.

(6) TMP80C50AU sorts the scores in magnitude order.

(7) The three highest scores and their word numbers are sent to host system I/F on TC8862F.

(8) The three highest scores and their word numbers are transferred to host system.

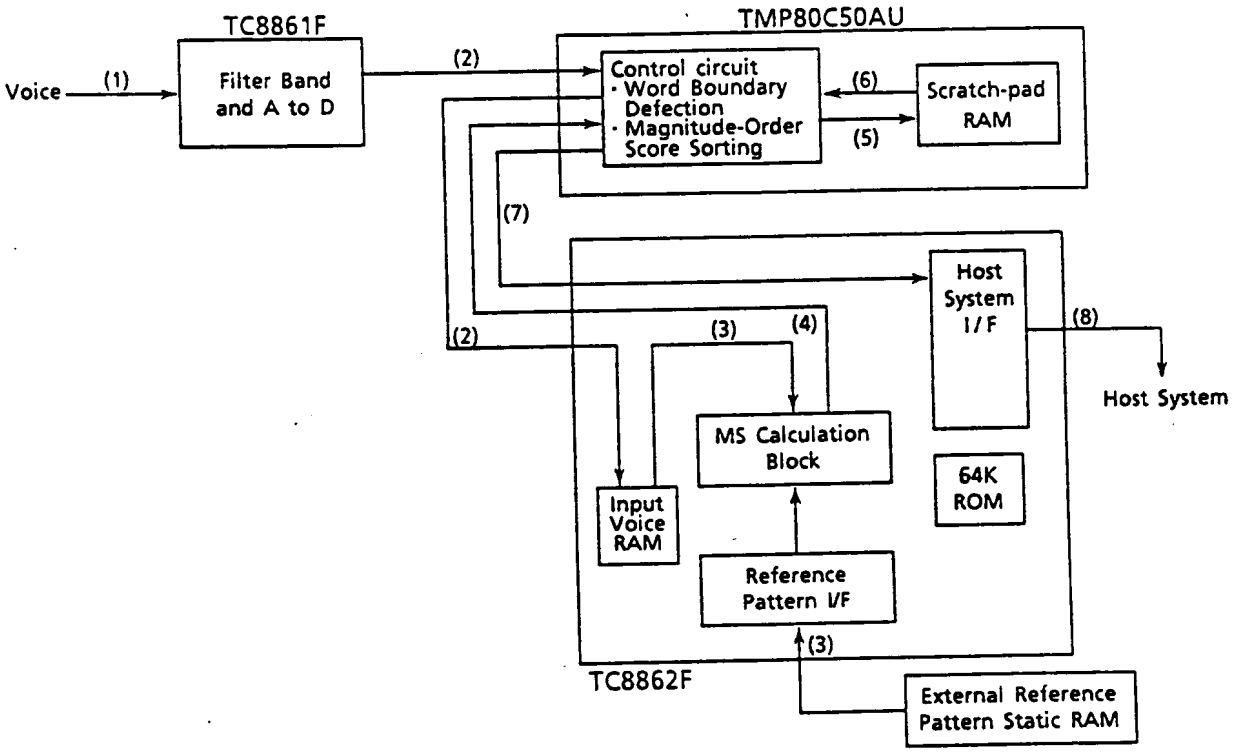


Fig. 4.3 Data Flow in Recognition

4.3 System State Transfer Chart

The device set changes its inner state by host-system command/data writing, host-system data reading and voice input through MIN/LIN terminals on TC8861F. The inner state transfer chart is depicted in Fig. 4.4. Here "writing" means command/data transfer from a host system to the device set and "reading" indicates data transfer from the device set to a host system.

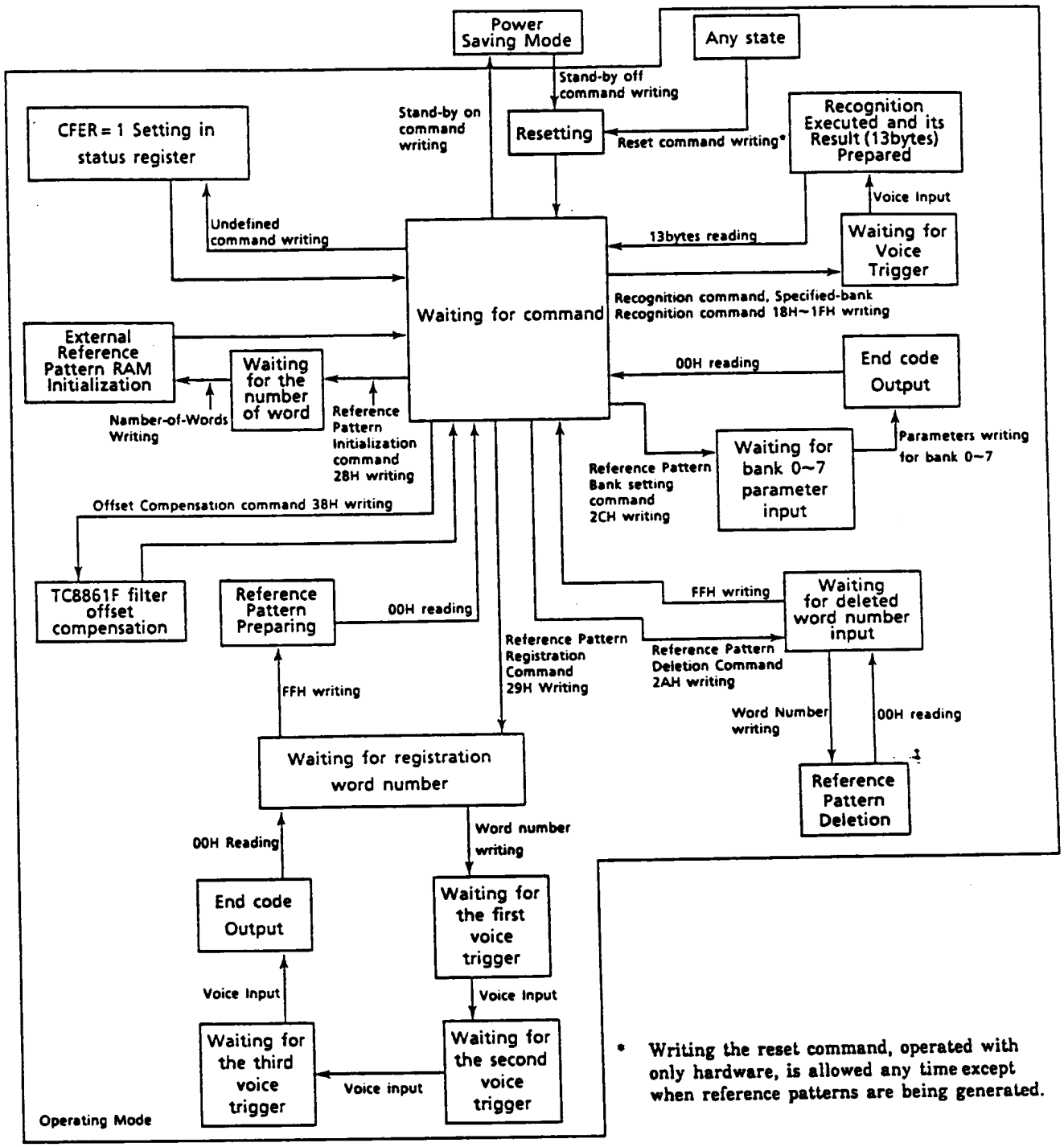


Fig. 4.4 System Inner State Transfer Chart

5. Host System Interface

5.1 Introduction to Interface Hardware

A host system operates the recognition device set with both commands and data transferred through the host system interface circuit on TC8861F. The circuit is designed to enable 8-bit parallel data bus to read or write, as implemented in a general-purpose 8bit parallel interface TMP82C55AP-5. The host system principally runs the device set in all the functions with reading or writing operations on 8bit data bus. TC8862F terminals used for the operations include HDB0~7, $\overline{HCS}$, $\overline{HRD}$, $\overline{HWR}$, HA0~1. Note that two additional terminals, HRRDY and HWRDY, alternative to the same named status flags in the status register, can be used to read out the device set state, if preferred in some cases. Functional description for the terminals are given in Table 5.1.

Table 5.1 Host Interface Terminals and their Functions

Terminal Names	Number of Terminals	Input/ Output	Description
HDB0~7	8	3 state Input/ Output	8 bit 3-state bidirectional data bus. Used for transferring commands, data and status between host system and device set.
$\overline{HCS}$	1	Input	Chip select input. At "L" level, data transfer with host system is enabled. At "H" level, all signals given by host system are ignored.
$\overline{HRD}$	1	Input	Read strobe signal. At "L" level, HDB0~7 is put in the output mode so that host system may read data on HDB0~7. (at $\overline{HCS}$ = HA1 = "L")
$\overline{HWR}$	1	Input	Write strobe signal. At rising edge, command or data are written from HDB0~7 into specific register. (at $\overline{HCS}$ = HA0 = "L")
HA1, HA0	2	Input	Addresses selecting command/data register, status register and reset/stand-by register. Generally connected to lower 2bits of address bus of host system.
HRRDY	1	Output	Host read ready signal. This terminal is placed at "H" level when data to be read by host system is available in TC8862F. As alternative, status register bit 0 also provides identical function.
HWRDY	1	Output	Host write ready signal. This terminal is placed at "H" level when host system is allowed to write into device set. Identical function is provided by status register bit 1.

5.2 Interface Hardware Configuration and its Timing

TC8862F host interface circuit hardware block diagram is illustrated in Fig. 5.1. The circuit contains three registers, command/data register (8bit), status register (8bit) and reset/stand-by register (1bit). Host system reading/writing operations with these registers run the device set. The registers are distinguished among themselves by two address terminals (HA0, HA1). The command/data register is enabled to be read/written and the status register is dedicated to reading only. The reset/stand-by register is dedicated to writing only.

Table 5.2 shows the terminal setting to realize the above-mentioned functions. Switching timings in reading or writing operations are illustrated in Fig. 5.3 and Fig. 5.4.

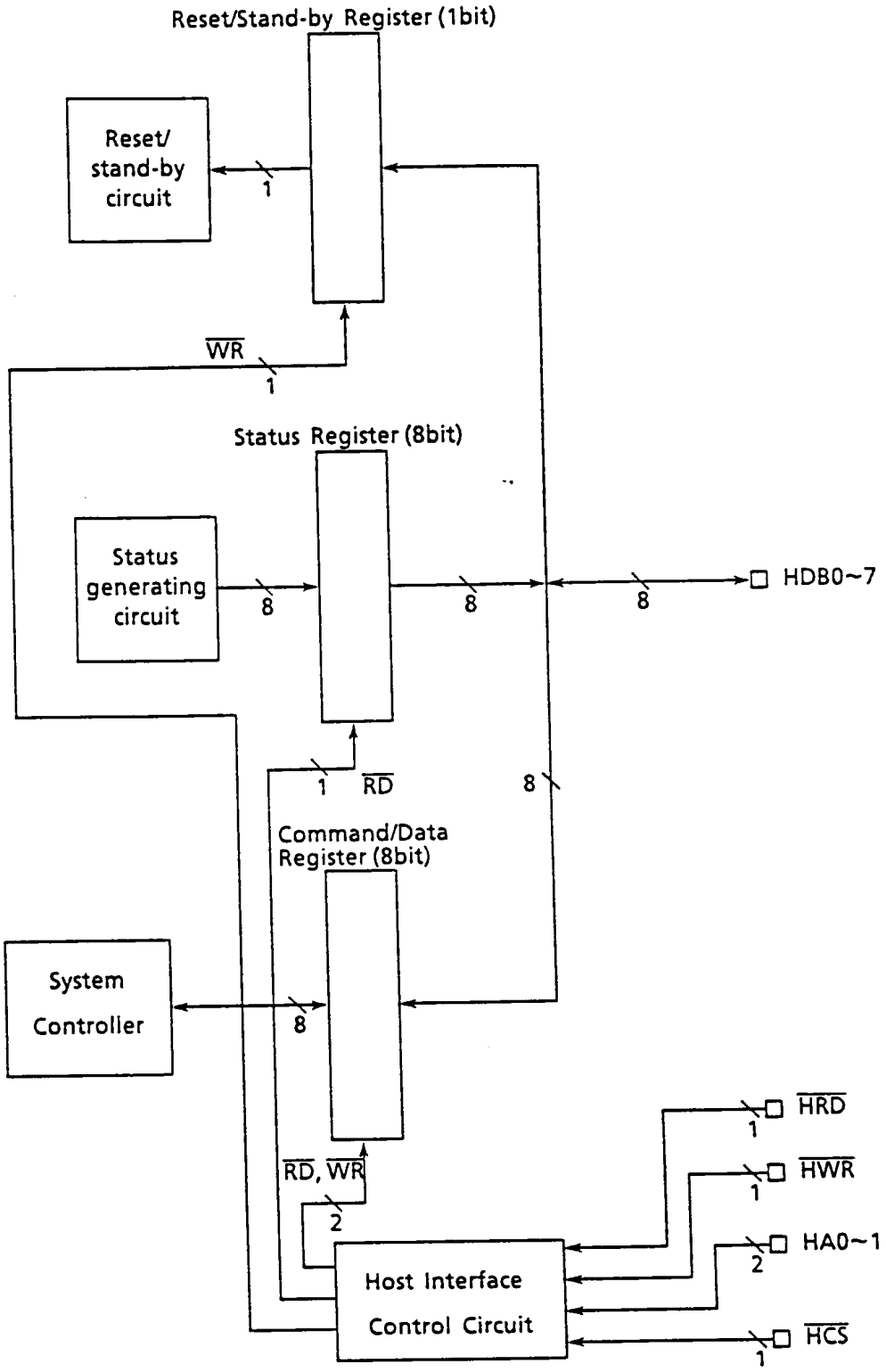


Fig. 5.1 Host Interface Circuit BlockDiagram

Table 5.2 Terminal Setting for Functions

HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	Functions
0	0	0	0	1	Data Reading.
0	0	0	1	0	Command/Data Writing.
0	1	0	0	1	Status Reading.
1	0	0	1	0	Reset/Stand-by Command Writing.
×	×	0	1	1	Device Set remains unchanged.
×	×	1	×	×	Device Set remains unchanged.
0	1	0	1	0	Device Set remains unchanged.
1	0	0	0	1	Device Set remains unchanged.
1	1	0	0	1	Device Set remains unchanged.
1	1	0	1	0	Device Set remains unchanged.
×	×	0	0	0	Not Allowed.

0 : "L" level
1 : "H" level
× : Don't care

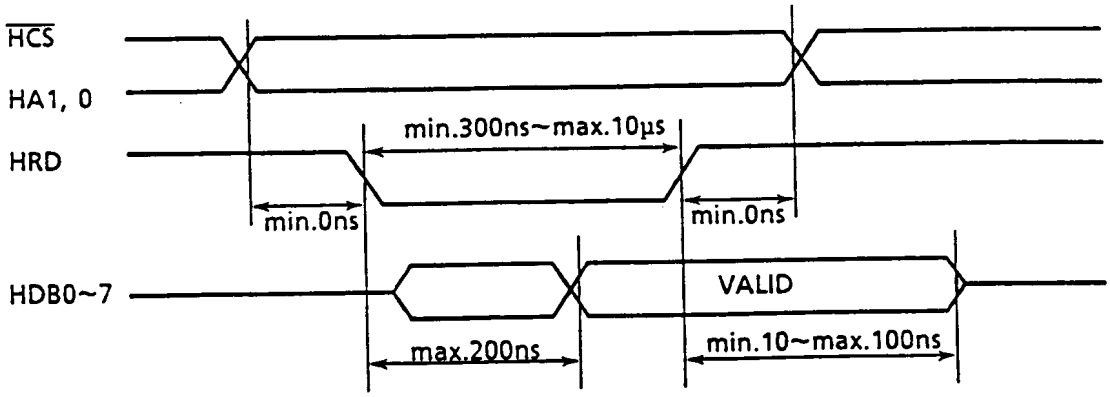


Fig. 5.2 Host Interface Reading Cycle Timing

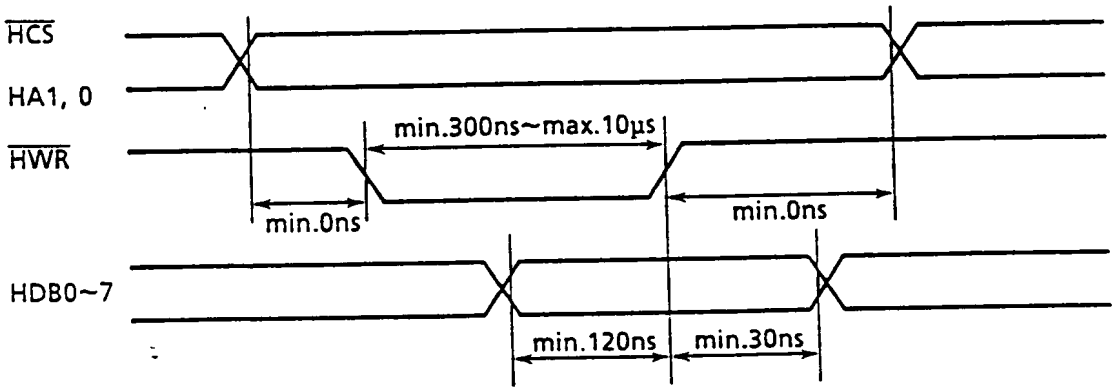


Fig. 5.3 Host Interface Writing Cycle Timing

5.3 How to Use Command/Data Register

Command/data register with 8bit data is used for "command"/"data" writing operation and data reading operation. Here "commands" are defined as 8bit data given into this register by a host computer on waiting state for the next command. On the other hand, "data" are defined as 8bit data transferred through the register while the device set is executing commands. Examples of "data" include "word number" given by a host system or "control code" output to a host system in registration command execution.

Table 5.3 shows a command list with the command/data register. Operating details and their usages are referred to 6.3 Command Description.

Table 5.3 Commands with Command/Data Register

Command	HDB0~7	HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$
Recognition	18H*	0	0	0	1	0
Reference Pattern Initialization	28H					
Reference Pattern Registration	29H					
Reference Pattern Deletion	2AH					
Reference Pattern Bank Setting	2CH					
TC8861F Filter Offset Compensation	38H					

* 18H is bank 0 recognition command. 19H is for bank 1. The same way holds for other banks. Namely 1AH is for bank 2 and 1FH is for bank 7. In case bank setting is not preset beforehand, only 18H executes recognition operation.

5.4 Hand Shake with Command/Data Register

Communication between the host system and the device set with the command/data register employs "hand shake" protocol. This protocol uses two status signals HRRDY (Host Read ReaDY) and HWRDY (Host Write ReaDY), offered as flag bits on the status register, or alternatively offered as device terminals.

HRRDY "1" indicates that the device set is ready to send some data to the host system while HWRDY "1" means that the device set is waiting for data to come from the host system. Note that the two status signals will not take "1" simultaneously.

Host system operational sequence is as follows:

(1) When commands/data are written into the device set,

① Check whether HWRDY "1".

② Write command/data into the device set when HWRDY is "1" (when the device set is waiting for command/data input). The finish of writing operation automatically leads to HWRDY "0". (The device set is released from the command/data waiting state.) Exit.

③ Go to ① when HWRDY is "0" (when the device set is not ready to receive command/data from the host system).

(2) When data are read out from the device set,

① Check whether HRRDY "1".

② Read data from the device set when HRRDY is "1" (when the device set is ready to output date to the host system). Reading operation automatically leads to HRRDY "0". (The device set is released from the sending-data ready state). Exit.

③ Return to ① when HRRDY is "0".

Fig. 5.4 illustrates the "hand shake" protocol timing diagram.

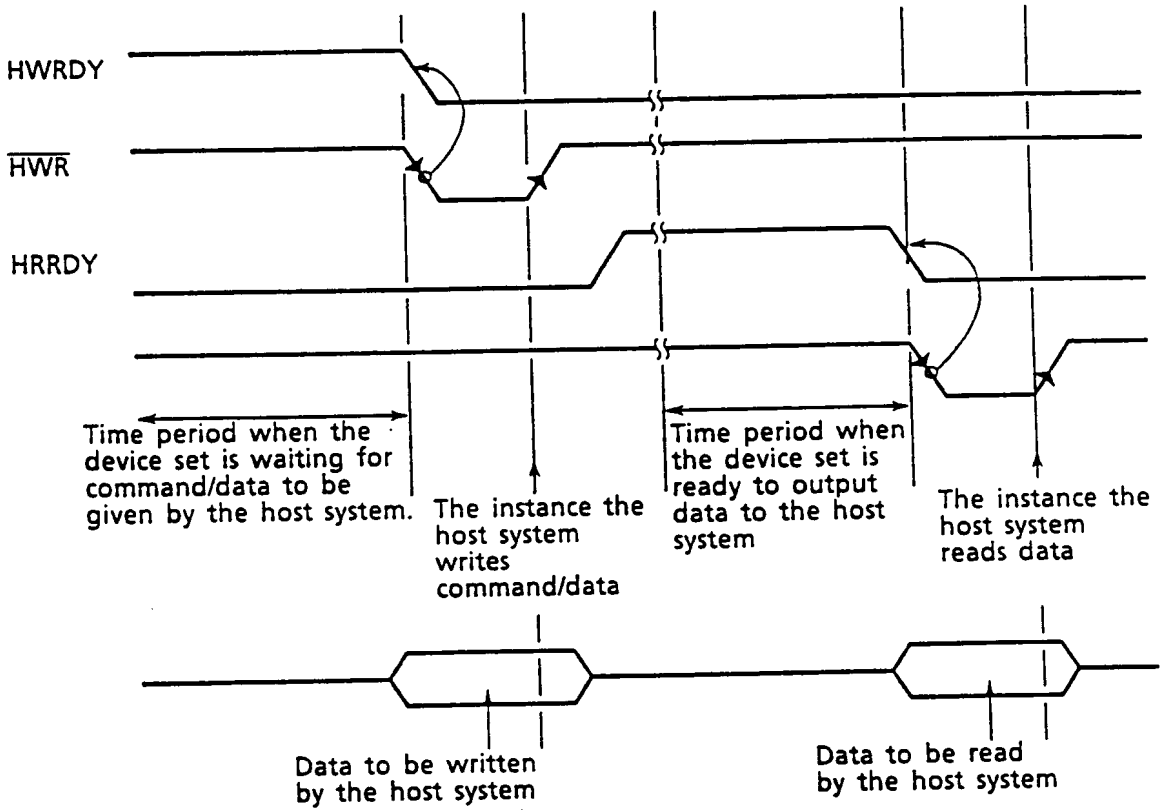


Fig. 5.4 "Hand Shake" Timing Diagram

5.5 How to Use Status Register

Status register with 8bit flags indicating the device set state is allowed only to be read. Reading operation don't requires the "hand shake" protocol described in 5.4. Instead reading is permitted in any instance. Each bit flag meaning is explained in the following figure.

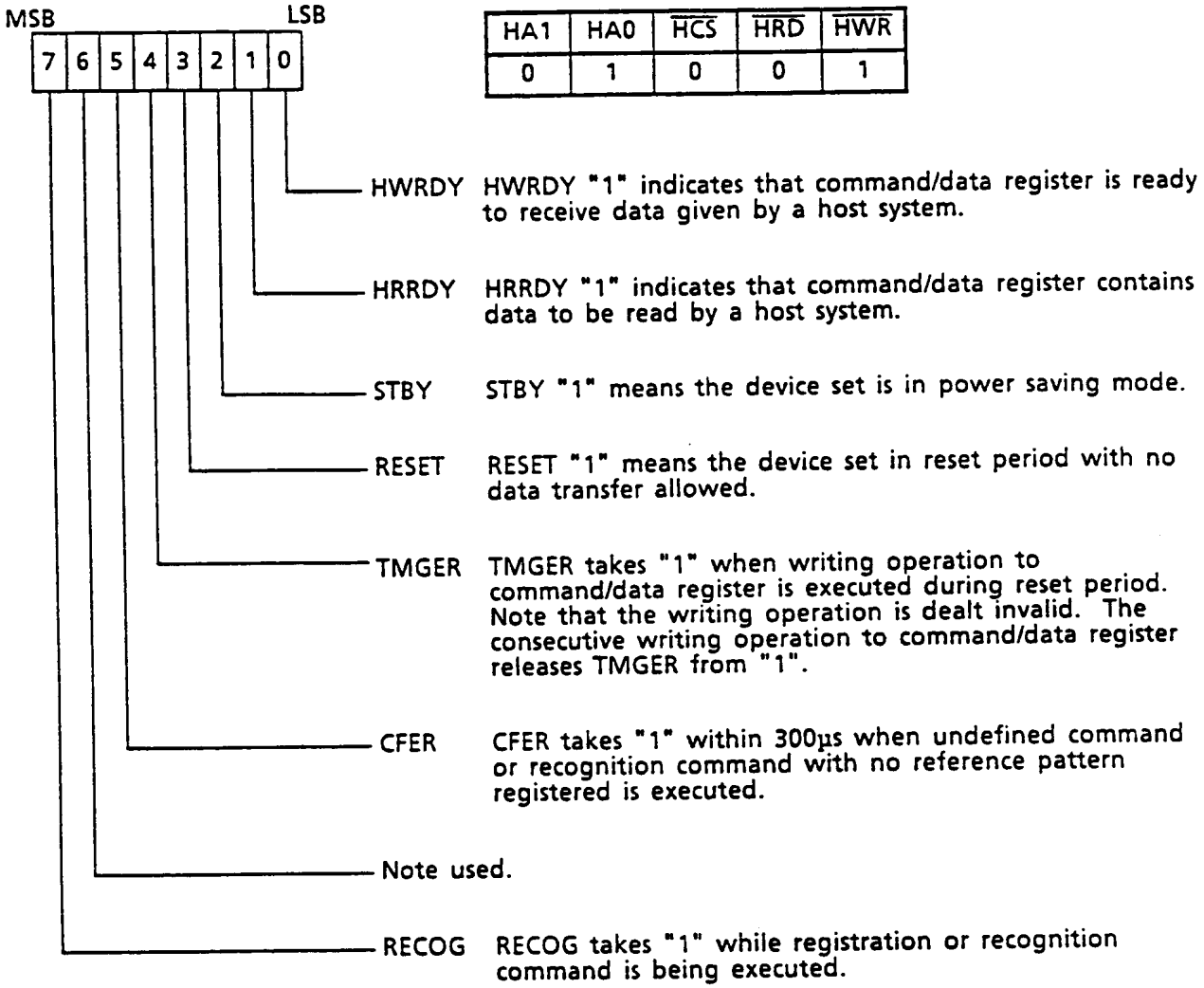


Fig. 5.5 Flag Meanings on Status Register

5.6 How to Use Reset/Stand-by Register

Reset/stand-by register with a 1bit writing-only flip-flop offers three kinds of functions determined by combination of the current device set state (power saving mode or operating mode) and 1bit datum, 0 or 1, to be written.

Writing with the least significant bit (LSB) of "0" (ex. 00H) to the reset/stand-by register in the operating mode results in reset command execution, which initializes the device set in hardware way and then returns it back to a waiting state for host system commands. Also writing with LSB of "1" (ex. 01H, FFH) in the operating mode leads to the power saving mode in the device set; which ceases all operations. Writing with LSB of "0" in the power saving mode releases the device set from the power saving mode to the operating mode.

Table 5.4 describes terminal settings and functions. Note that writing to the reset/stand-by register do not require the "hand shake" protocol described in 5.4, and is allowed to be executed any time.

Table 5.4 Reset/stand-by Register Function

HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	HD0 (LSB)	Description	The Device Set State on Writing
1	0	0	1	0	0	Reset the device set	Operating Mode
1	0	0	1	0	1	Place the device set in power saving mode	Operating Mode
1	0	0	1	0	0	Release the device set from power saving mode	Power Saving Mode

6. Host System Command

The device set always operates with commands given by a host system. This chapter overviews how to write programs on a host system for the device set management. 6.1 shows an example of host system operation as introduction. 6.2 describes commands acceptable to the device set. 6.3 handles detail explanations to use commands. 6.4 depicts all data formats employed in the device set.

6.1 Host System Operation Flow Chart Example

Here described is a flow chart example to operate the device set in the following sequence:

(1) Reference pattern initial registration for five words.

(2) Recognition.

(3) Reference pattern deletion for one word.

These three activities are essential to any recognition device. Fig. 6.1 illustrates the flow chart. Operation in the flow chart is generally realized by a tip of hardware and tens of steps in software. More details in each operation in Fig. 6.1 are referred to 6.3.

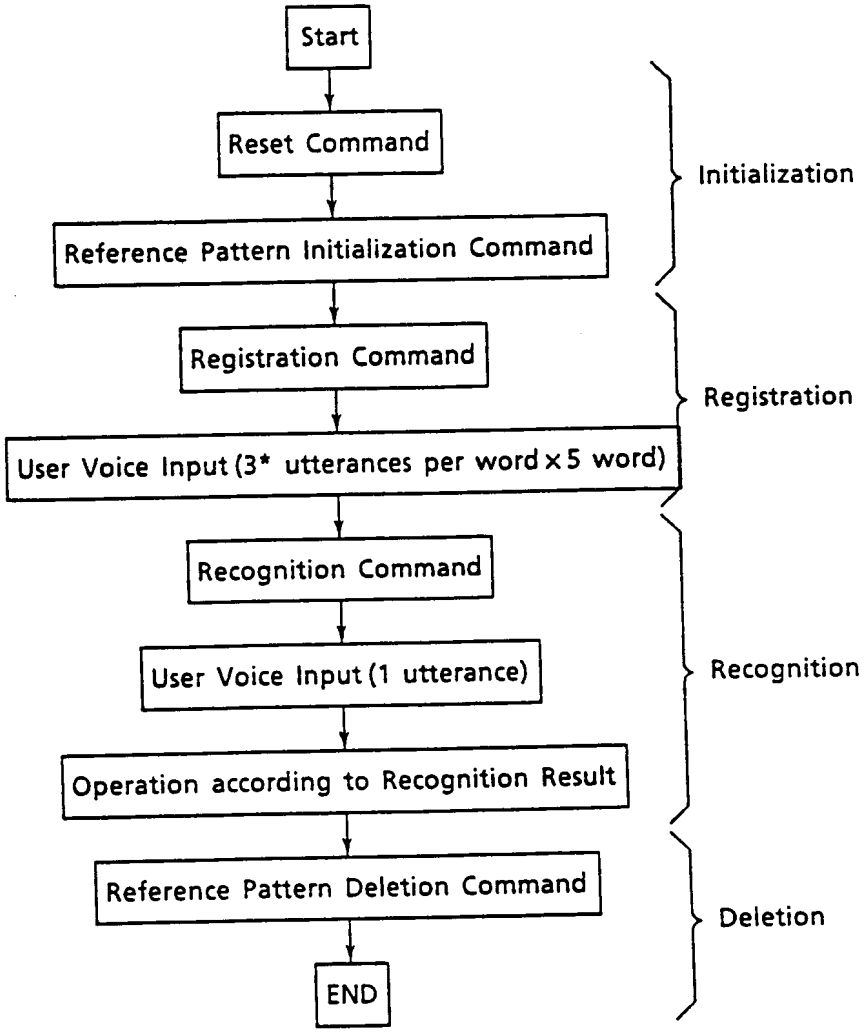


Fig. 6.1 Host System Operation Flow Chart Example

* More than 3 utterance per word may be required in some cases.
See details in 6.3.2 Reference Pattern Registration Command.

6.2 Command List

All commands available are listed in Table 6.1.

These commands are 8bit data written into the device set by a host system. The commands are divided into two categories, one employing command/data register and the other using reset/stand-by register.

Table 6.1 Command List

Command Name	HDB0~7	HA1	HA0	$\overline{HCS}$	$\overline{HRD}$	$\overline{HWR}$	Notes
Reference Pattern Initialization	28H	0	0	0	1	0	Command/data Register used
Reference Pattern Registration	29H	0	0	0	1	0	
Reference Pattern Deletion	2AH	0	0	0	1	0	
Reference Pattern Bank Setting	2CH	0	0	0	1	0	
TC8861F Filter Offset Compensation	38H	0	0	0	1	0	
Recognition (78 word)	18H*	0	0	0	1	0	
Reset	HDB0 = 0	1	0	0	1	0	Reset/stand-by Register used
Stand-by On	HDB0 = 1	1	0	0	1	0	
Stand-by Off	HDB0 = 0	1	0	0	1	0	

* Recognition commands other than 18H are valid as described in the following table in case reference pattern bank is created beforehand.

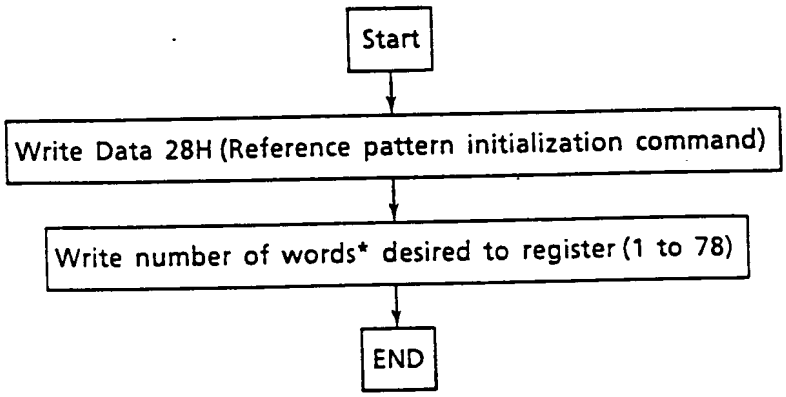
Bank 0 Recognition	18H	$HA1 = HA0 = \overline{HCS} = \overline{HWR} = 0$ $\overline{HRD} = 1$
Bank 1 Recognition	19H	
Bank 2 Recognition	1AH	
Bank 3 Recognition	1BH	
Bank 4 Recognition	1CH	
Bank 5 Recognition	1DH	
Bank 6 Recognition	1EH	
Bank 7 Recognition	1FH	

6.3 Command Description

This section describes a host system operational flow chart for each command.

6.3.1 Reference Pattern Initialization Command

Reference pattern initialization command initializes reference patterns and CPU scratch-pad memory so that it may enable the device set to be ready to initial registration. This command should be executed once after power supply to the device set is turned on. The Fig. 6.2 illustrates the host system operational flow chart for the command. Note that the number of words desired to register in the chart is less than or equal to the maximum number of words calculated from reference pattern RAM capacity.



* Since the device set controller (TMP80C50AU) does not examine the validity of value written as the number of words, the host system program must guarantee it. Otherwise the proper operation since then can not be assured.

Fig. 6.2 Reference Pattern Initialization Command Flow Chart

6.3.2 Reference Pattern Registration Command

This command registers voice features on reference pattern RAM segments designated by word numbers. It allows multiple of words to be registered in its single execution. Fig. 6.3 shows the flow chart for a host system. After registration command (29H) is written to command/data register, the device set asks for a word number to be registered. When the word number is written, usually three utterances per word are required to be input through analog input terminal on TC8861F. In some cases where similarity among the spoken three is low, another three utterances for the word is required. Writing "FFH" as a word number starts arithmetic operations to create reference patterns and then output a registration end code (a kind of control code) at their completion. Reading the code leads the device set to the state waiting for another command. The arithmetic operations for more number of words stored require more processing time. Typical processing time is 9 seconds for 30 words, and 32 seconds (max. 34 seconds) for 78 words.

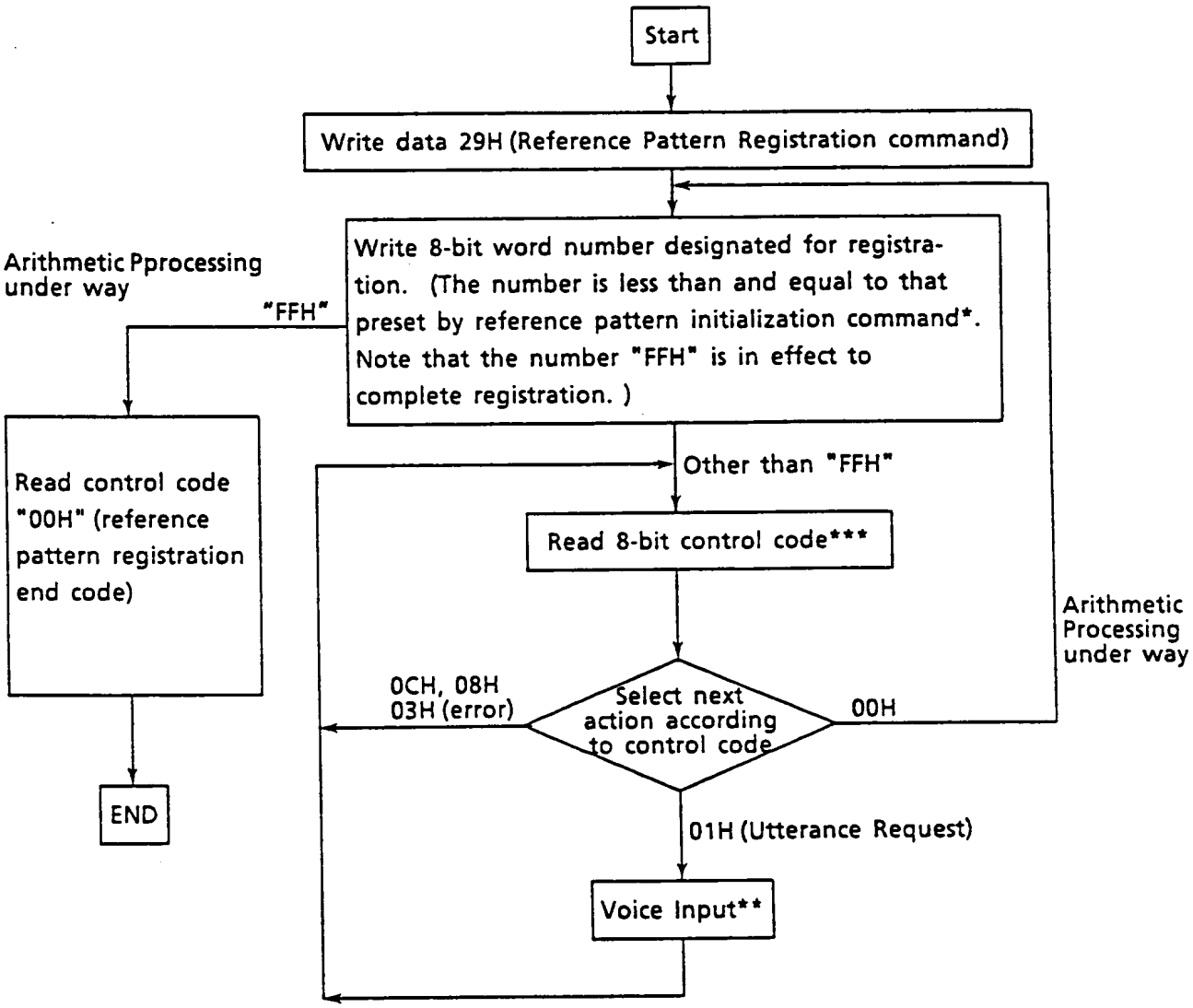


Fig. 6.3 Reference Pattern Registration Command Flow Chart

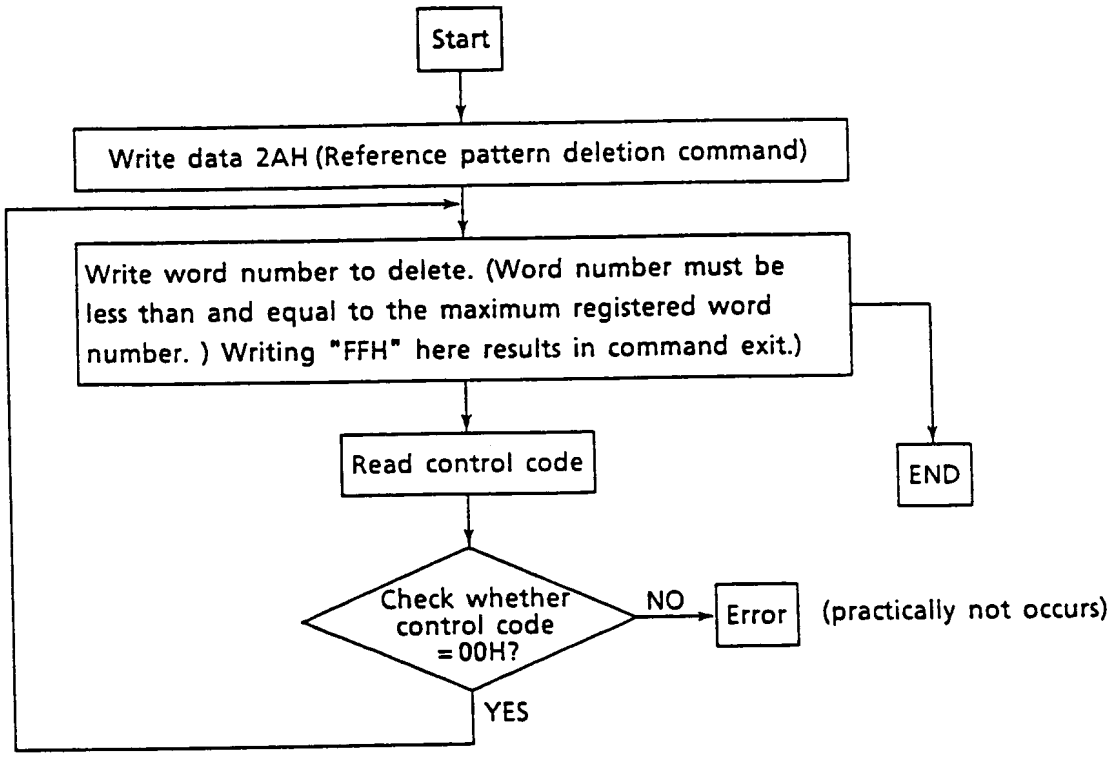
* Since the device set does not examine the validity of value written as a word number, a host system should guarantee it. Wrong value input will lead to malfunction.

** Three utterances per word are principally required. However more than three utterances are required in the case where similarity among the first three is low.

*** Meanings of control codes are referred to 6.4.3 Control Code List.

6.3.3 Reference Pattern Deletion Command

Reference Pattern Deletion command clears into zero reference pattern data of a specified word. Word numbers and their reference patterns of words other than the specified remains unchanged.



6.3.4 Reference Pattern Bank Setting Command

This command specifies how many consecutive words are included in 8 different banks. It must be executed at least once before specified-bank recognition commands (19H~1FH) are operated. The command may be written any multiple times but the newest setting is always valid.

Reference pattern bank setting command and specified-bank recognition command is a complementary pair for functions with banks. Bank setting command assigns 8 groups of consecutive word numbers to 8 banks. Specified-bank recognition command uses those bank numbers in order to recognize input voice as one of words in designated banks when input voice is previously known as one of them.

The device set uses up to 8 banks. Every bank must be set in terms of the number of consecutive words in the bank setting command even if only some of 8 are used. For instance, when only 3 banks are used, the other 5 must also be set to "0" as the number of words respectively possessed. On the other hand specified-bank recognition command execution for a bank with no word specified leads the device set, without any recognition activity, to waiting-command state with CFER bit "1" in status register.

If the total sum of the 8 numbers of words for 8 banks exceeds 78, the device set returns other than "00H" as a control code (a return code). Also the current bank setting is of no effect, and the previous bank setting is preserved.

If the total sum exceeds the maximum registered word number, specified-bank recognition copes with words of up to the maximum registered word number.

On the contrary, if the total sum comes less than the maximum registered, recognition commands deals with only words included by 8 banks.

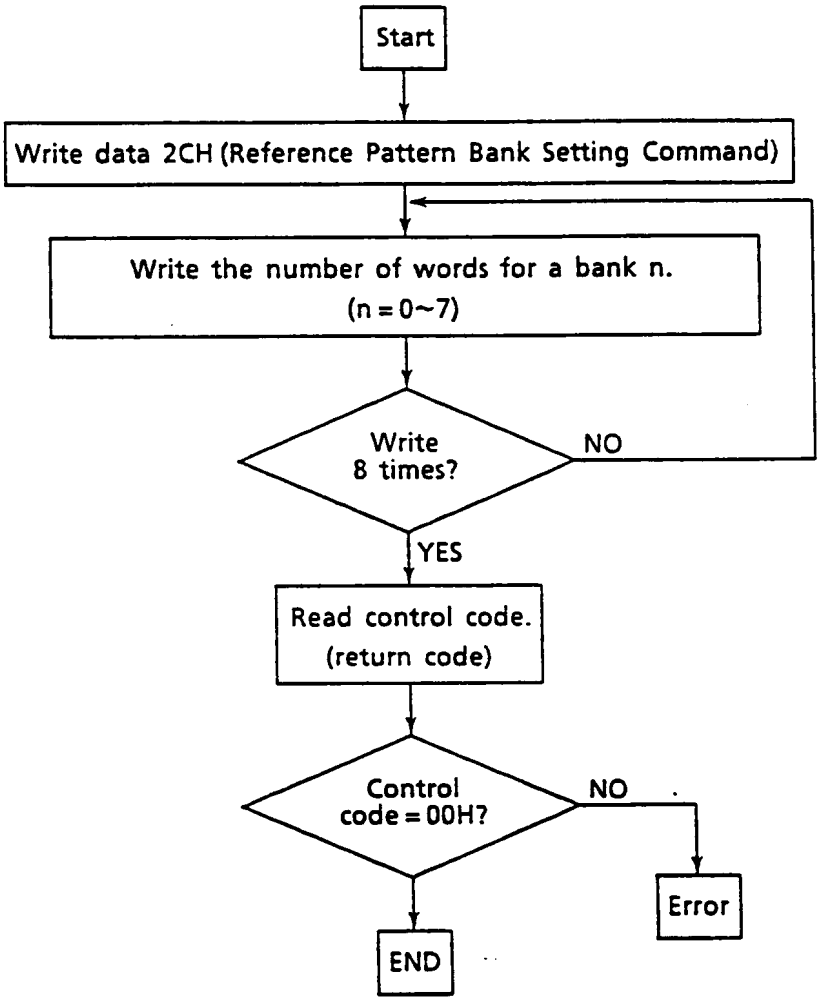


Fig. 6.5 Reference Pattern Bank Setting Command Flow Chart

6.3.5 TC8861F Filter Offset Compensation Command

The command compensates for TC8861F filter offset.

Offset values vary by individual TC8861F or its assembly condition. Offset degrades frequency analysis accuracy on TC8861F and then reduces recognition performance. To eliminate this harmful influence, TC8861F is equipped with offset compensation function. The command executes the function on TC8861F. This function is automatically executed every time the reset command or stand-by on command is operated or when power supply is turned on. However users are recommended to execute this command explicitly at about 5 minute interval in case the device set is operated continuously for more than 5 minutes without any interruption by either the reset command or the stand-by on command.

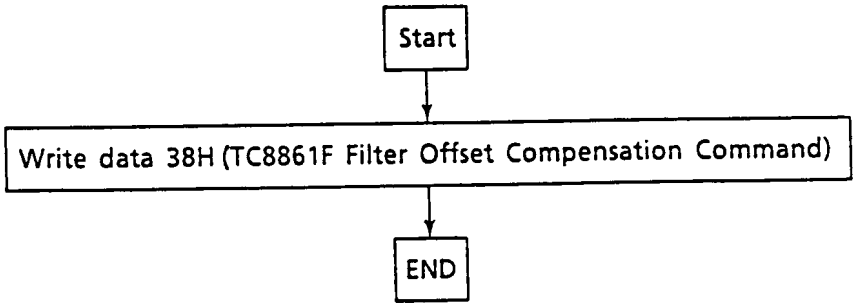
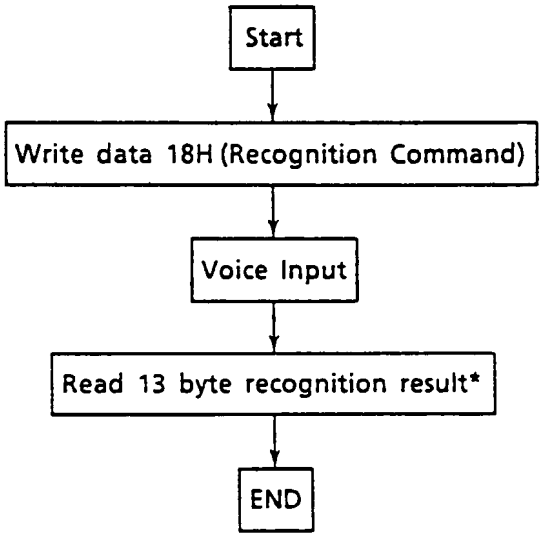


Fig. 6.6 TC8861F Filter Offset Compensation Command Flow Chart

6.3.6 Recognition Command

The command performances recognition of input voice on vocabulary reference patterns registered by reference pattern registration command. Recognition result consisting of 13byte data returns back to a host system.

If the reference patterns don't exist (the case happens if any registration has not been executed after reference pattern initialization), the recognition command does not proceed any longer and results in command waiting state with status register CFER bit "1".



* Refer to 6.4.1 Recognition Result Data Format

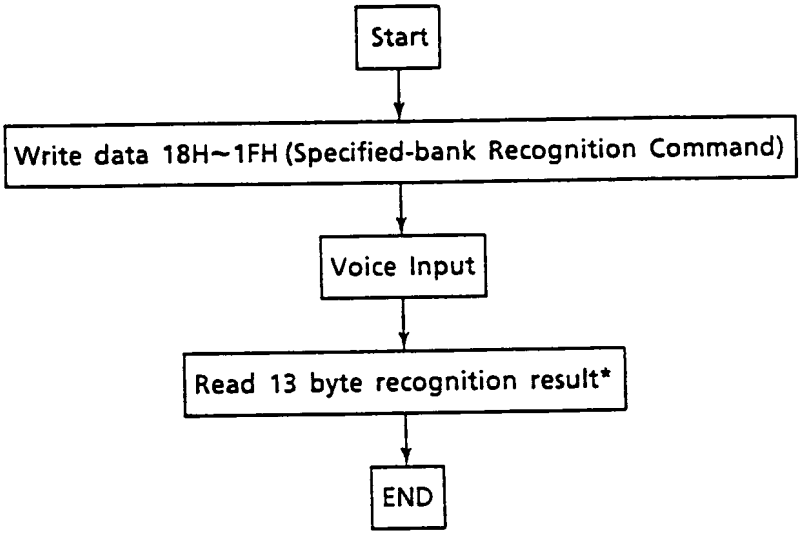
Fig. 6.7 Recognition Command Flow Chart

6.3.7 Specified-Bank Recognition Command

The device set is equipped with recognition on banks of reference patterns. Specified-bank recognition requires reference pattern bank settings previously performed by reference pattern bank setting command.

The recognition command for bank 0 is 18H, one for bank 1 is 19H, one for bank 2 is 1AH, and one for bank 7 is 1FH.

When bank setting has not be performed after power supply on, all reference patterns registered are treated as involved in bank 0. In this case only recognition command 18H is valid and other specified-bank recognition command 19H~1FH are of no effect.



* Refer to 6.4.1 Recognition Result Data Format

Fig. 6.8 Specified-Bank Recognition Command Flow Chart

6.3.8 Reset/Stand-by Command

(1) Reset Command, Stand-by Off Command.

Reset command is used to release the device set from hung-up state to normal operation state if it happens. It is also operated as stand-by off command to release the power saving mode when the device is in the mode. In both cases it initializes the device set in such a way that the device set saves all previous data in its scratch-pad RAM and its reference pattern RAM. Actual actions are as follows. The command

- Initializes all registers on each device.
- Clears all flags on each device.
- Resets program counter (PC) on TMP80C50AU to 000H and then starts program from PC=000H.
- Compensates for TC8861F filter offset.
- Leads the device set to command waiting state.

During these reset command action, status register flag RESET keeps "1". So a host system operates as described below.

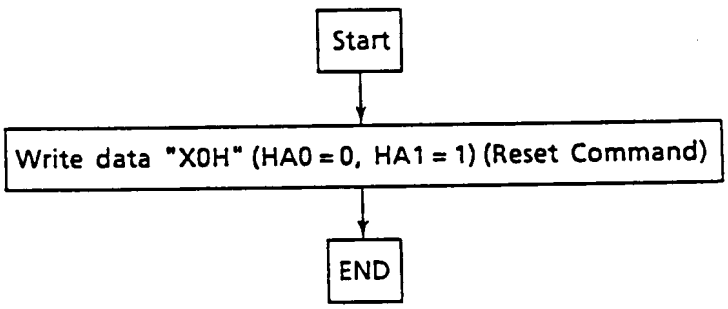


Fig. 6.9 Reset Command Flow Chart

(2) Stand-by On Command

Stand-by On Command leads the device set to power saving mode, where TC8861F, TC8862F and TMP80C50AU hold their system CK to realize total device set power supply current less than 10μA. The command allows the device set to preserve their system parameters on both internal RAMs and external reference pattern RAMs. The mode can be detected by status register flags STBY=1 and RESET=1. Note that RESET flag is also 1 in the power saving mode. Stand-by off command releases the device set from power saving mode.

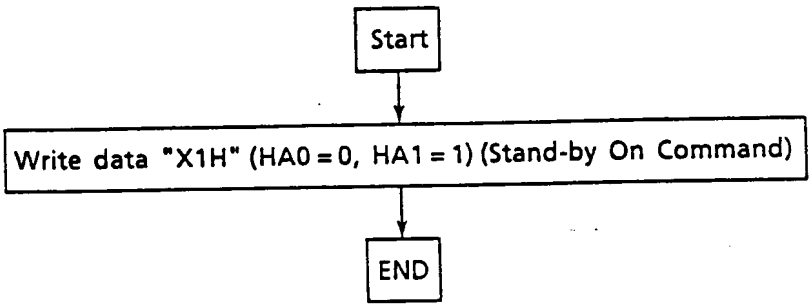


Fig. 6.10 Stand-by On Command Flow Chart

(3) Reset Timing (HA1=1, HA0=0, $\overline{HCS}$=0)

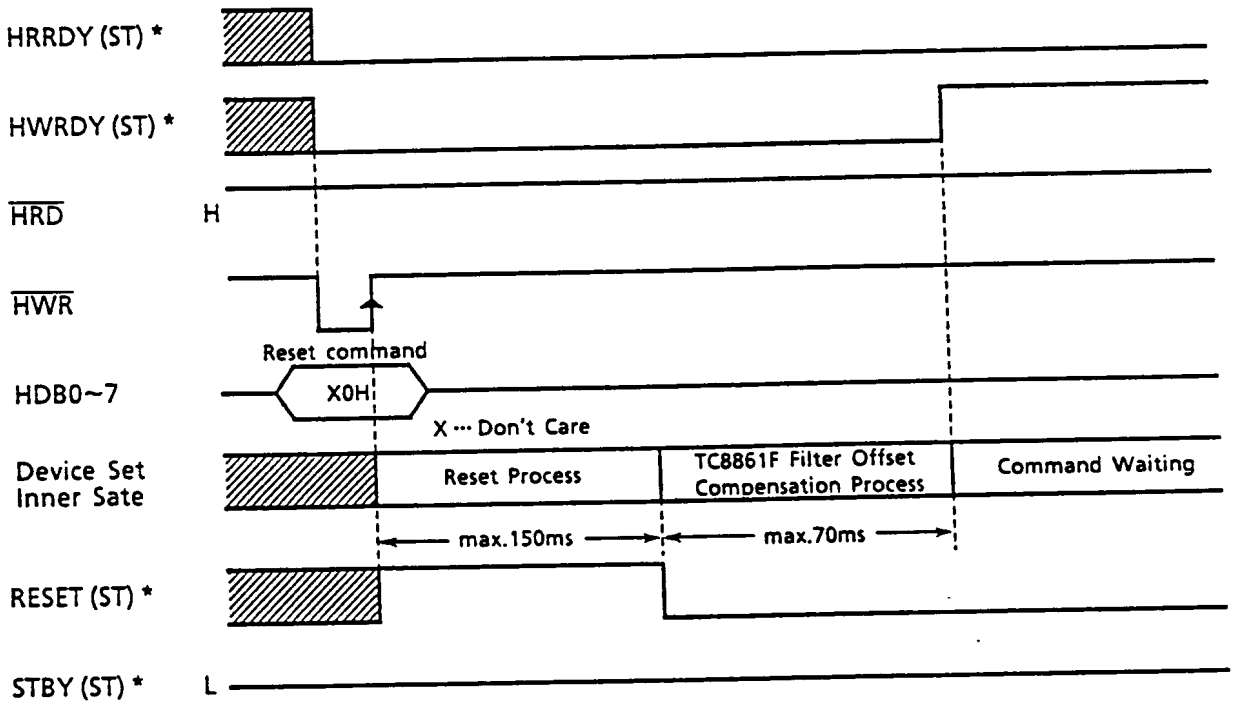


Fig. 6.11 Reset Command Timing Diagram

* ST means a status bit on the status register.

(4) Stand-by on/off Timing (HA1=1, HA0=0, $\overline{HCS}$=0)

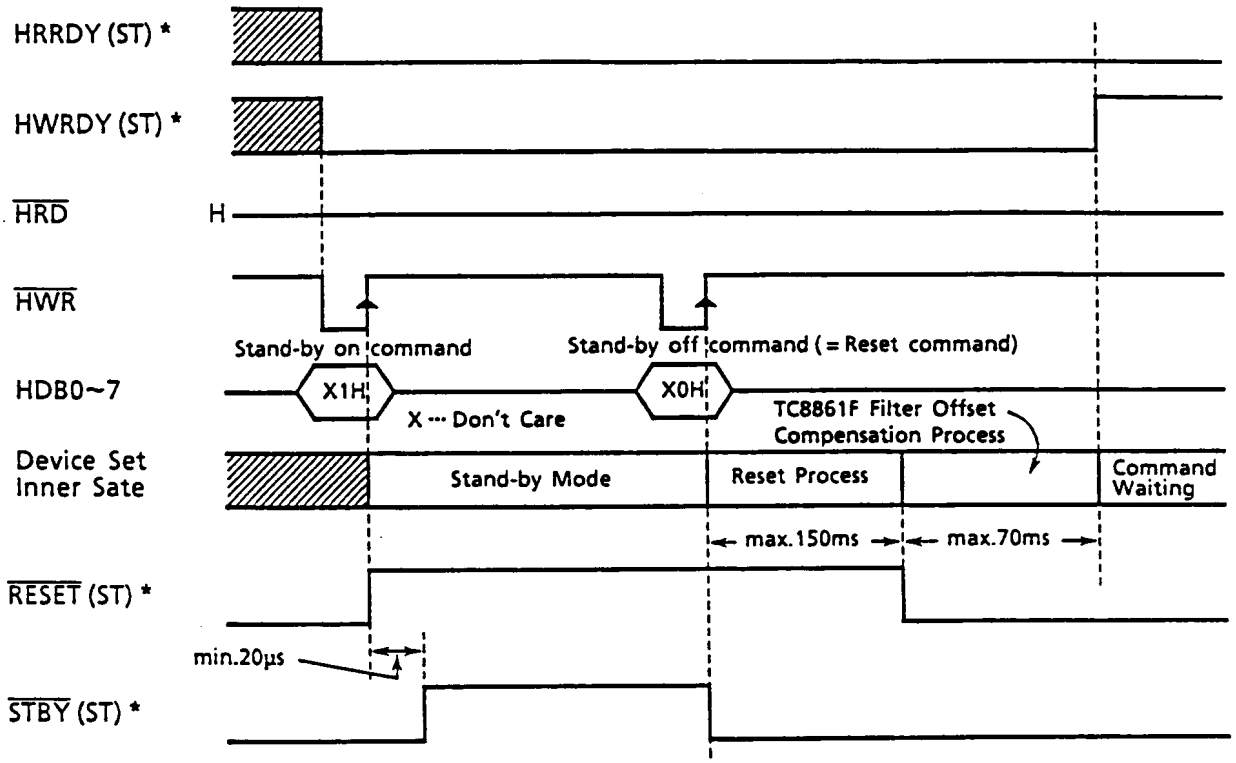
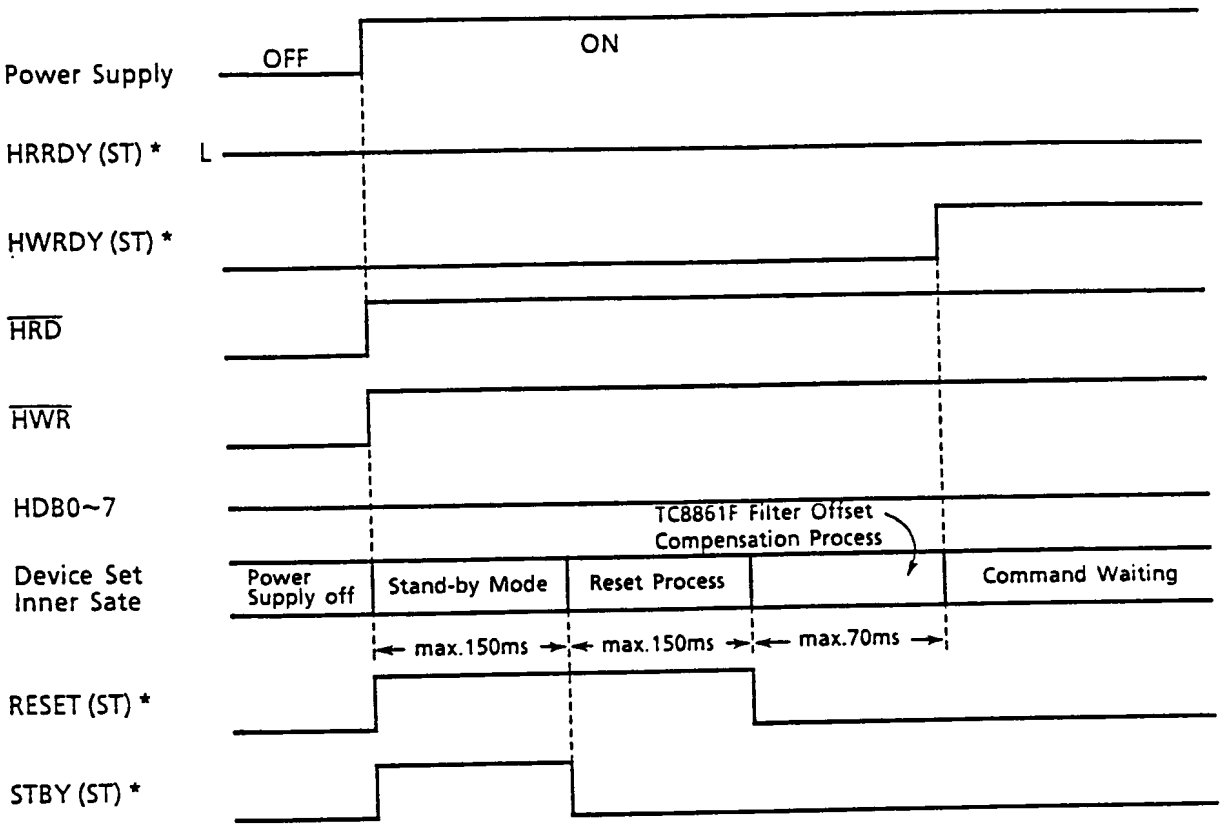


Fig. 6.12 Stand-by On/Off Command Timing Diagram

* ST means a status bit on the status register.

(5) System Transition Timing When Power Supply Turns On



* ST means a status bit on the status register.

Fig. 6.13 Transition Timing Diagram When Power Supply Turns On

Execute reset command once for complete system initialization when power supply turns on.

6.3.9 Notes on Reset Command Usage

With a single exception stated below, a host system can operates reset command any time even when the device set performs a certain process. The process interrupted by reset command still allows following commands to operate with previous device-set operation history alive, because the process can preserves essential system parameters of scratch-pad RAM and reference pattern RAM safely.

This data preservation capability provided by he reset command offers convenience to handle the device set in various applications. Several examples includes cases where a host system intends to;

(1) Quit voice input waiting state in recognition command or reference pattern registration command forcefully when the voice will not come in.

(2) Quit infinite loops of recognition command, if it happens.

(3) Stop processes on their way driven by wrong commands.

(4) Recover from hung-up state in host computer program development.

Unique exception is the time period for actual arithmetic calculation in reference pattern registration command. Execution of rest command must be prohibited in the time period between writing FFH and reading control code (end code). There actual arithmetic calculation for reference patterns is performed from three utterances per word and the reference patterns are transmitted to external SRAM. If it is nevertheless executed in the prohibited period, none of reference patterns is guaranteed.

However, as long as the reset command is executed in periods other than the prohibited even during reference pattern registration command, reference patterns to be developed since now as well as those already prepared can be restored completely. The following paragraph explains sequences to restore patterns.

If rest command enters before "FFH" as word number is input, sets of three utterances per word just already spoken are still alive in the scratch-pad memory. But the problem is that reference patterns for the words are not completed yet because actual arithmetic calculation is suspended due to reset operation. To complete them, the second registration command must be executed on command waiting state immediately after the reset command execution. On the first prompt for word number entry in the second registration command, writing "FFH" must be operated to execute actual arithmetic calculation with those utterances spoken in the first registration command.

6.4 Data Format

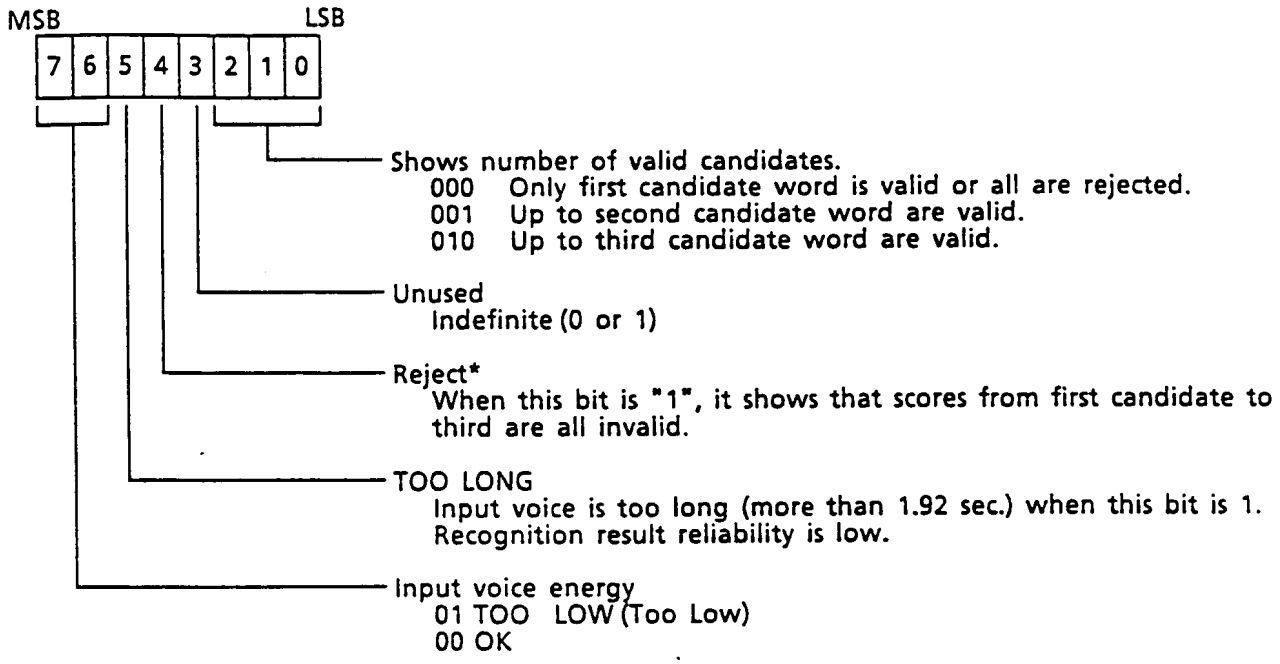
6.4.1 Recognition Result Data Format

Recognition Result Header (Refer to description in the next page)	
First Candidate Word Number	
Second Candidate Word Number	
Third Candidate Word Number	
First-Candidate Word Similarity Score	(Lower Byte)
First-Candidate Word Similarity Score	(Middle Byte)
First-Candidate Word Similarity Score	(Upper Byte)
Second-Candidate Word Similarity Score	(Lower Byte)
Second-Candidate Word Similarity Score	(Middle Byte)
Second-Candidate Word Similarity Score	(Upper Byte)
Third-Candidate Word Similarity Score	(Lower Byte)
Third-Candidate Word Similarity Score	(Middle Byte)
Third-Candidate Word Similarity Score	(Upper Byte)

13 Byte Data

Fig. 6.14 Recognition Result Data Format

6.4.2 Recognition Result Header Format



* Reject Flag "1" indicates reliability of recognition result is low.

Fig. 6.15 Recognition Result Header Format

6.4.3 Control Code List

Table 6.2 Control Code List

Value	Meaning
00H	Input voice is normal.
01H	Utterance of word is requested.
03H	Second or third utterance has much difference from first for word in registration mode, thus correct reference pattern of the word can not be made.
08H	Input voice is too long (more than 1.92 sec.)
0CH	Input voice is too low in energy.

6.4.4 Structure of Reference Patterns

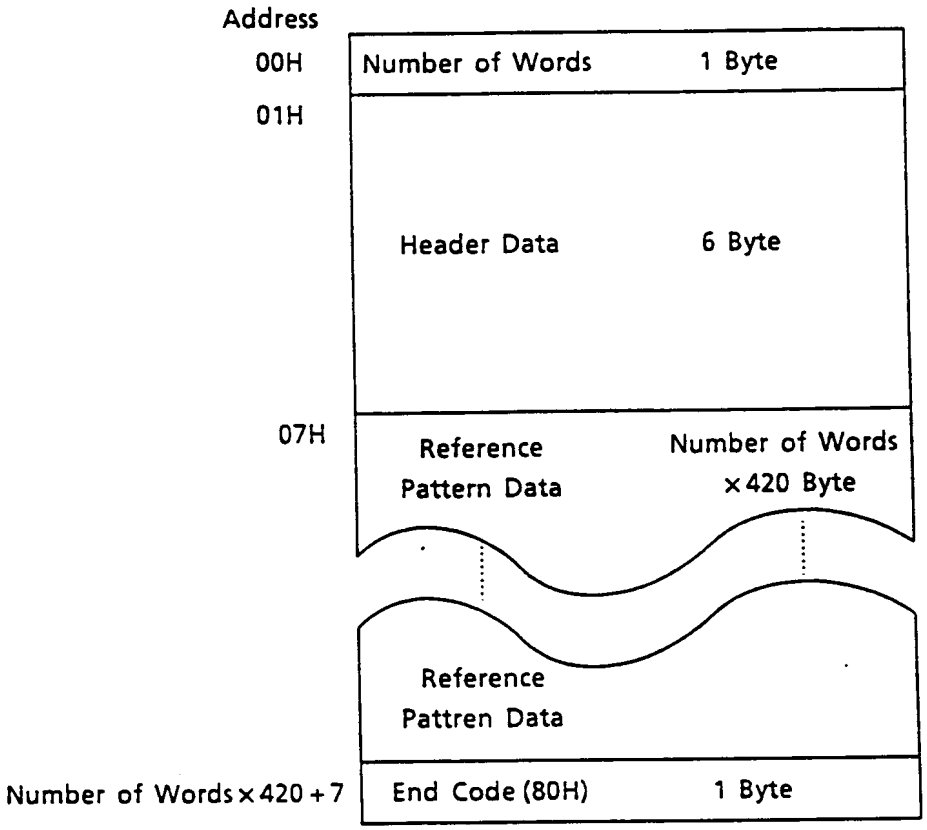


Fig. 6.16 Reference Pattern Format

7. Application Circuitry Example

Host CPU: Z80

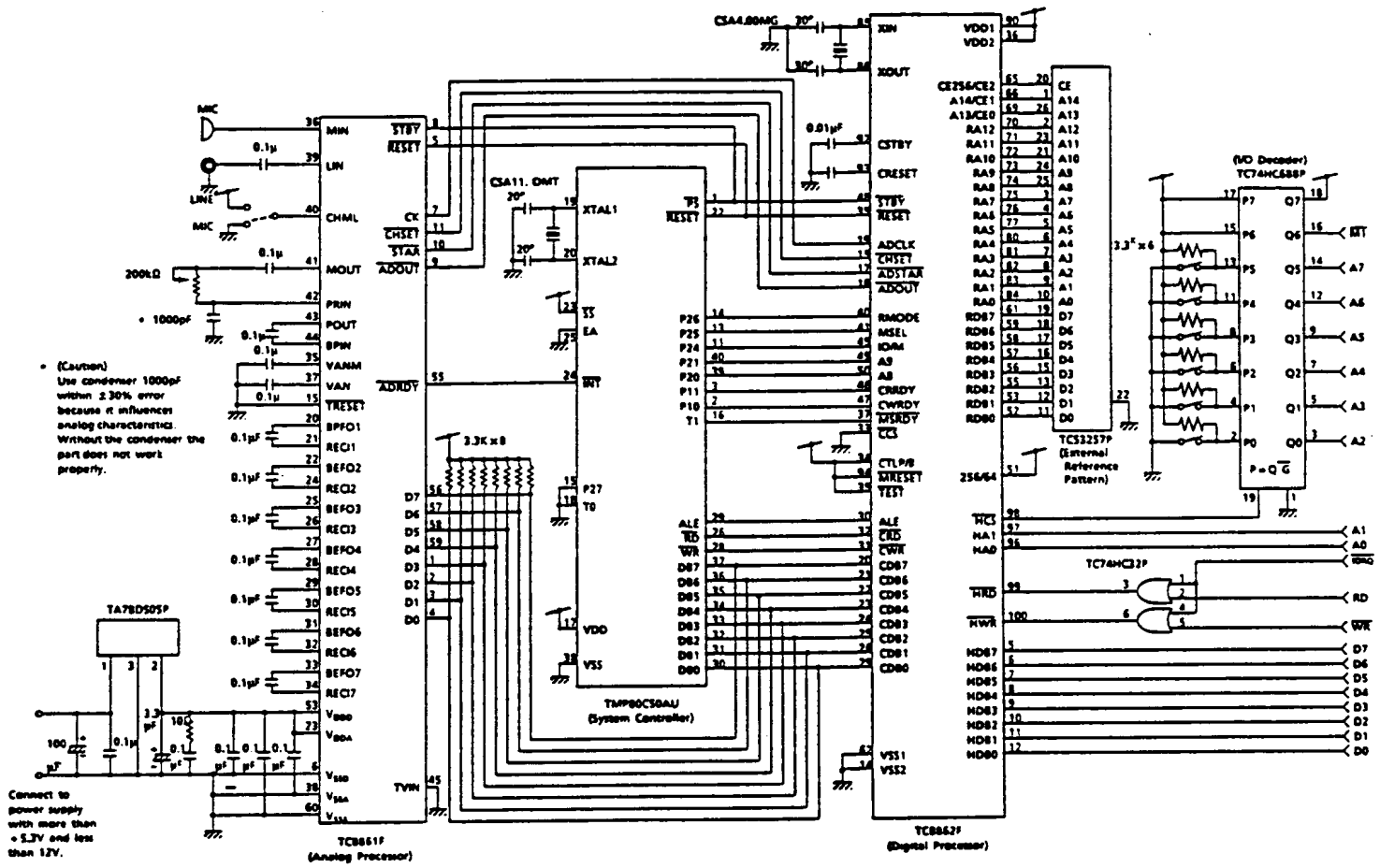


Fig. 7.1 Application Circuitry Example

8. Detail Description on Each Device

8.1 TC8861F (Acoustic Processing Analog Device)

8.1.1 Functional Description and Block Diagram

The device performs acoustic processing for analog voice input signal to prepare acoustic feature extraction parameters. The block diagram is presented in Fig. 8.1 and signal processing flow is described in following paragraph.

Analog voice signal fed through either MIN terminal or LIN terminal is amplified first in either a microphone amplifier (Gain=26dB) or a line amplifier (Gain=15dB) and then is amplified again in a preamplifier. The preamplifier gain can vary by a variable resistor (RVI) from 0 dB (RVI=450kΩ) to 20 dB (RVI=0kΩ). The amplified signal is then fed to HPF to emphasize high frequency for consonant power level amplification. Next, the signal is input into 7 channel filter bank to perform frequency analysis. Each filter bank channel consists of a supplementary low pass filter (LPF), a band pass filter (BPF), a rectifier and a smoothing low pass filter. The supplementary LPF and the BPF extracts a portion of signals lying in pass-band of frequency range between fL and fH shown in Fig. 8.1 BPF block.

Then the rectifier rectifies the BPFed signal in absolute manner and the smoothing LPF (cut frequency=50Hz) smooths the rectified signal. Therefore the output from the smoothing LPF represents averaged amplitude time series of waveform in pass-band frequency region uniquely determined for each filter channel.

Single analog-to-digital converter (A to D) digitizes 7 outputs of smoothing LPFs in time serial manner by selecting only one at once with a multiplexer. The A to D digitizes each channel time series at time intervals of 20msec. The input-output digitizing characteristic in the A to D shows non-linearity with 8bit compressed output. Analog input signal full range for the A to D is approximately 2 (V).

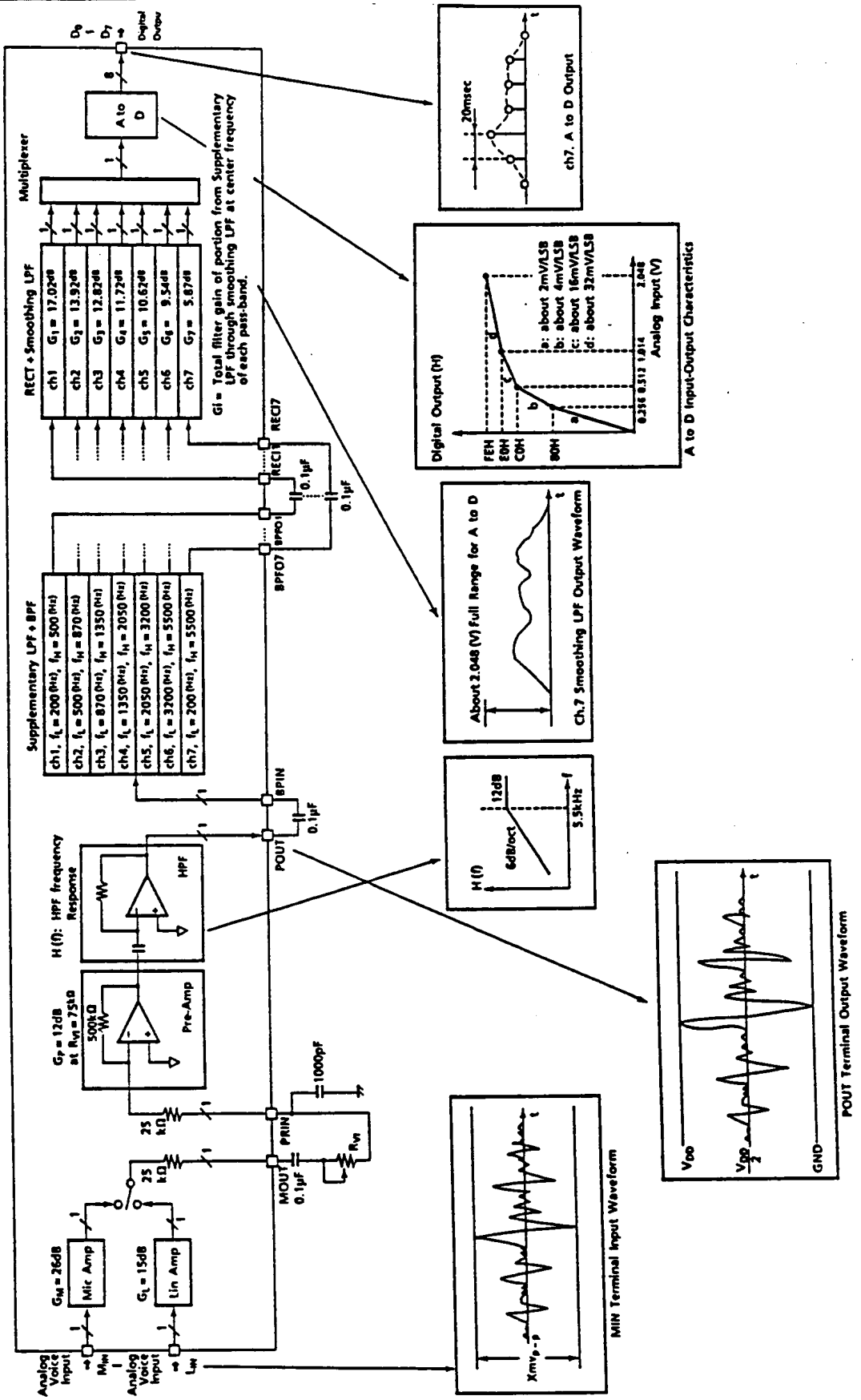


Fig. 8.1 TC8861F Block Diagram

8.1.2 TC8861F Pin Assignments

MFP 60 PIN

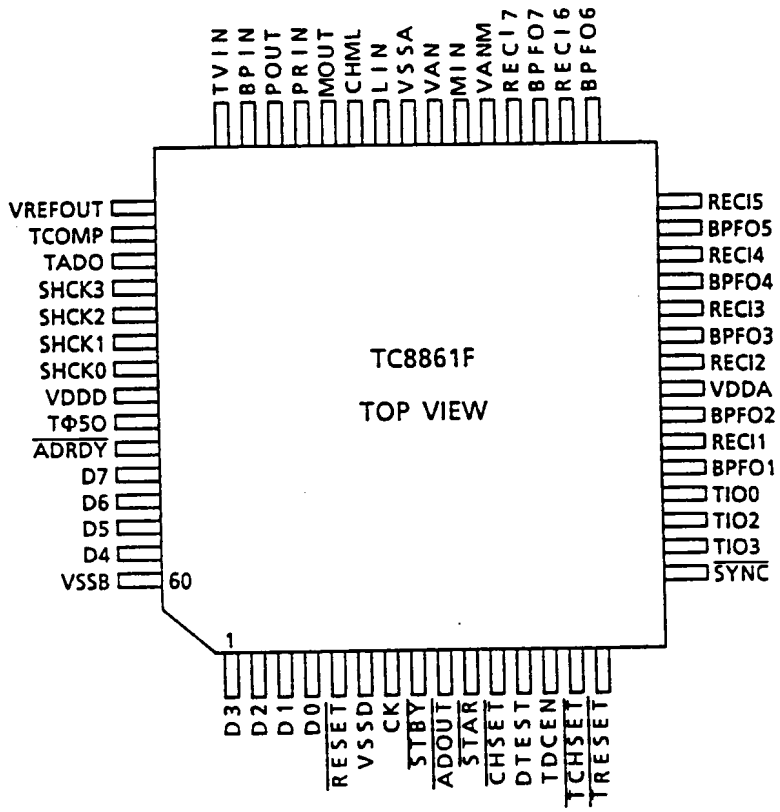


Fig. 8.2 TC8861F Pin Assignment Diagram

8.1.3 TC8861F Signal Description

(1) D0 ~ D7 (Data bus) [Input/Output]
8-bit bidirectional data bus. To be connected to the inner bus of the recognition system. These terminals are used by TMP80C50AU to write data into TC8861F and read data from TC8861F.

(2) $\overline{\text{CHSET}}$ (CHannel SET strobe) [Input]
When L to H rising signal is input to this terminal, D0-D7 data (To select multiplexer input filter channel) is written in the internal register of TC8861F. This terminal is connected to the $\overline{\text{CHSET}}$ terminal of TC8862F.

(3) $\overline{\text{ADOUT}}$ (A to D read OUT strobe) [Input]
When L level signal is input to this terminal, D0-D7 become the output mode and data (A to D output data) of the output register on TC8861F is output on D0-D7. This terminal is to be connected to the $\overline{\text{ADOUT}}$ terminal of TC8862F.

(4) $\overline{\text{STAR}}$ (a to d STARt signal) [Input]
A to D conversion start signal to A to D converter to be connected to the $\overline{\text{ADSTAR}}$ terminal of TC8862F.

(5) CK (ClocK) [Input]
Clock input terminal. By being connected to the ADCLK terminal of TC8862F, system clock (Typ. 2MHz) is supplied from TC8862F.

(6) $\overline{\text{RESET}}$ (system RESET) [Input]
Reset input terminal. To be connected to the $\overline{\text{RESET}}$ terminal of TC8862F. When L level signal is input to this terminal, TC8861F is reset.

(7) $\overline{\text{STBY}}$ (STand-BY) [Input]
Stand-by input terminal. To be connected to the STBY terminal of TC8862F. When L level signal is input to this terminal, TC8861F is put in the stand-by state. At this time, however, the RESET terminal must have been set at L level in advance.

(8) $\overline{\text{ADRDY}}$ (A to D ReaDY) [Output]
This terminal is H level when the A to D converter is in the conversion operation and is L level after end of the conversion. This terminal is to be connected to the $\overline{\text{INT}}$ terminal of TMP80C50AU.

(9) MIN (Microphone INput) [Input]
Microphone signal input terminal. A microphone can be directly connected. When the CHML terminal is at L level, this terminal is input to TC8861F. The microphone signal ground level must be equal to Vss (ground) level of LSI.

(10) LIN (Line INput) [Input]
Line input terminal. Voice signal is input to this terminal through the coupling capacitor. When the CHML terminal is at H level, this terminal is input to TC8861F.

(11) CHML (CHange input terminal between Min and Lin) [Input]
Control signal to select whether a signal to be processed by TC8861F is input signal from the MIN terminal or that from the LIN terminal.

(12) MOUT (Min/lin amplifier OUTput) [Output]
Output terminal of the MIN or LIN input amplifier selected by the CHML terminal. To be connected to the PRIN terminal through a capacitor and a variable resistor.

(13) PRIN (PReamplifier INput) [Input]
Preamplifier input terminal. Output signal from the MOUT terminal is input to this terminal. A capacitor 1000PF (deviation within ±30%) is to be placed between this terminal and Vss (Ground) level in order to stabilize analog characteristics. Without the capacitor TC8861F does not operate properly.

(14) POUT (Preamplifier OUTput) [Output]
Preamplifier output terminal. To be connected to the BPIN terminal through a capacitor.

(15) BPIN (Band-Pass-filter INput) [Input]
Band-pass filter input terminal. Output signal from the POUT terminal is input to this terminal.

(16) VAN (Voltage level of ANalog ground) [Output]
Ground level of analog signal on analog circuit expect the MIN amplifier. To be connected to the system ground (Vss) through a capacitor.

(17) VANM (Voltage level of ANalog ground for Mic amplifier) [Output]
Ground level of analog signal on the MIN amplifier. To be connected to the system ground (Vss) through a capacitor.

(18) VREFOUT (Voltage level of REFerence OUTput for A to D) [Output]
Reference voltage monitor terminal for A to D converter.

(19) BPF01~BPF07 (Band-Pass-Filter Output) [Output]
Output terminals for 7 band-pass filters. These terminals are respectively to be connected to the rectifier input terminals (RECI1-7) correspondent to each channel.

(20) RECI1~RECI7 (RECtifier Input) [Input]
Input terminals of 7 rectifiers.

(21) TIO0, TIO2, TIO3 (Test Input/Output) [Input/Output]
Test input/output terminals. Nothing should be connected to this terminal.

(22) TVIN [Input]
Test input terminal.
Set at L level. (Connect to the system ground Vss.)

(23) $\overline{\text{SYNC}}$, $\overline{\text{TREST}}$, $\overline{\text{TCHSET}}$, TDCEN, DTEST/TDCSET, TAD0 [Input]
Test input terminal with pull-up or pull-down resistor. Nothing should be connected to this terminal.

(24) TΦ50, TCOMP [Output]
Test output terminal. Nothing should be connected.

(25) SHCK0~SHCK3 (Sample & Hold ClocK) [Output]
Test output terminal. Nothing should be connected.

(26) VDDD, VDDA
VDDD is the TC8861F digital circuit power supply terminal. VDDA is the TC8861F analog circuit power supply terminal. Both should be connected to the plus side of the power supply.

(27) VSSD, VSSB, VSSA
Ground terminals. VSSD is for TC8861F digital circuit, VSSB is for TC8861F data bus buffer and VSSA is for TC8861F analog circuit.

8.1.4 Method to Wire External Miscellaneous Parts

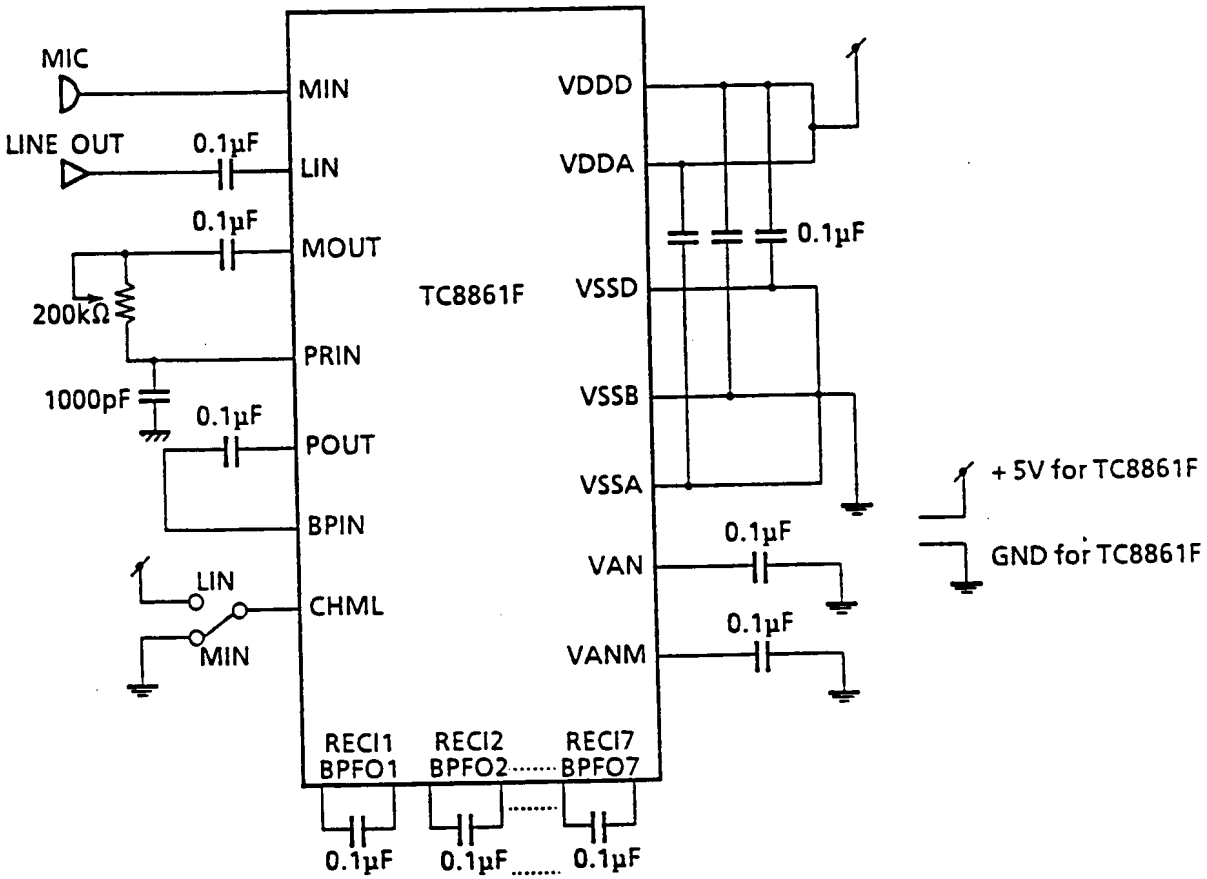


Fig. 8.3 Wiring Diagram

Because TC8861F is an analog device, special care must be taken of wiring external parts to maintain its analog characteristics. Following cautions must be carefully observed.

(1) Employ either MIN or LIN as an input terminal so that input voice may always pass through either microphone amplifier or line amplifier. The reason is that filter offset calibration offered by the device requires one of them to be passed through by input signal. Otherwise the calibration not performed properly will lead to degradation in recognition accuracy.

(2) Position a bypass capacitor 0.1μF between power supply pins (VSS-VDD) as closed to the pins as possible. Total 3 capacitors should be placed between VDDD-VSSD, VDDD and VSSB, and VDDA and VSSA.

(3) Position VAN and VANM level stabilization capacitors close to the pins.

(4) Use shield wires or pattern wires guard-ringed by GND against disturbing noise for MIN and LIN terminals.

(5) Place parts between MOUT and PRIN, POUT and BPIN, BPFOi and RECIi (i=1~7) as close to the pins as possible and connect them to the pins with short wires.
Warning! Place certainly a preamplifier stabilizing capacitor 1000PF within ±30% deviation between PRIN and VSSA as close to the pins as possible. Otherwise the device will not operate properly.

8.1.5 Method to Adjust Voice Level

Adjustment of voice level is important to maintain the device set high recognition performance. Two different stage adjustment are recommended to be employed.

(1) Variable Resistor (RVI) Setting: Adjustment by waveform amplitude on POUT.

Appropriate resistance setting on variable resistor (RVI) is usually once required when the device set is implemented in application product. RVI setting covers deviations in operational circumstance factors such as sensitivity microphone, distance between mouth and microphone, and signal to Noise Ratio on MIN or LIN. Therefore it should not usually be done more that once after device set installation.

Concrete explanation about the setting is presented in the following: The criteria of appropriate setting is offered in such a way that maximum waveform amplitude of voice on POUT with analog GND 1/2 VDD (VDD: Supply power voltage) is equal or slightly more than full-range of GND-VDD. Although slight clipping of the signal on POUT due to a little louder voice do no harm, both too much clipping due to extremely loud voice and too little waveform due to too small voice reduces recognition performance.

An experiment with Japanese word "HAI", meaning "YES" in English, shows an equation about relationship between RVI value R (kΩ) and MIN or LIN maximum waveform amplitude X (mVp-p) or Y (mVp-p) producing full-range waveform on POUT as follows:

On MIN Terminal:

$$X\,(mVp\text{-}p) = 70\,(mVp-p) \times \frac{\frac{500k\Omega}{75k\Omega+50k\Omega}}{\frac{500k\Omega}{R+50k\Omega}} = 70\,(mVp-p) \times \frac{4}{\frac{500k\Omega}{R+50k\Omega}}$$

On LIN Terminal:

$$Y\,(mVp\text{-}p) = 70\,(mVp-p) \times \frac{4}{\frac{500k\Omega}{R+50k\Omega}} \times \frac{20\,(times)}{5.6\,(times)}$$

Table 8.1 indicates value relationships between R and X or between R and Y. Note that values indicated in the table are standard and will vary by factor 2 according to vocabulary.

Table 8.1 Relationship of values between R and X or between R and Y

R (kΩ)	X (mV_{p-p}) on MIN Terminal	Y (mV_{p-p}) on LIN Terminal
0	28	100
25	42	150
75	70	250
125	98	350
175	126	450
450	280	1000

Evaluation experience recommends around 15kΩ as R for condenser microphone.

(2) Input Voice Energy Flag in Recognition Result Header

Input voice energy flag mainly covers voice level deviation of individual utterance given by personal characteristics, like male or female. The flag is embedded in a 1byte recognition result header returned to host system on recognition command execution. (See 6.4.2 Recognition Result Healer Format.) Upper 2bits of the header categorize the level of voice just recognized in two stages (too low, OK). Indication of this 2bit information to users helps better input voice level setting for next recognition.

8.1.6 Threshold for Word Boundary Detection

Word boundary detection threshold is used to determine valid voice signal period. Input signals with level exceeding the threshold, lasting over a certain period of time, is picked up as valid voice. The detection is followed by pattern matching activity.

The device set adaptively determines the threshold by monitoring background noise level when no voice exists, and changes the threshold level from '4H' (about 8mV) through '20H' (64mV) according to background noise. It sets lower threshold for lower background noise and higher threshold for higher background noise.

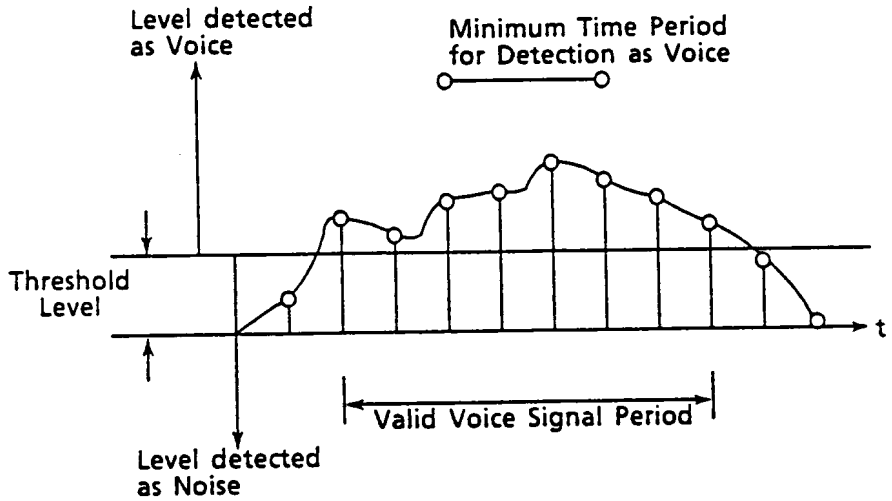


Fig. 8.4 Word Boundary Detection Scheme

8.1.7 Remarks on Power Supply

Since TC8861F is an LSI with the analog circuit built in, its analog characteristics may be adversely affected by the noise of a power supply. In order to prevent mixing of noise, observe the following cautions:

- Separate a power supply to TC8861F from that to other LSI's (TC8862F, TMP80C50AU, Host System and other LSI's). (2 power supplies)
- GNDs of two power supplies should be connected at only one point. Furthermore, that connecting point should be close to the supplies. This will minimize the effect of noise from the other power supply GND to the power supply GND of TC8861F.
- The power supply for TC8861F should have as less ripple as possible and a series regulator power supply is recommended for best condition. If a switching regulator power supply is used, it should be stabilized by a three-terminal regulator. An example of a circuit, when a power supply is composed of a combination of a switching regulator power supply and a three-terminal regulator, is shown below.

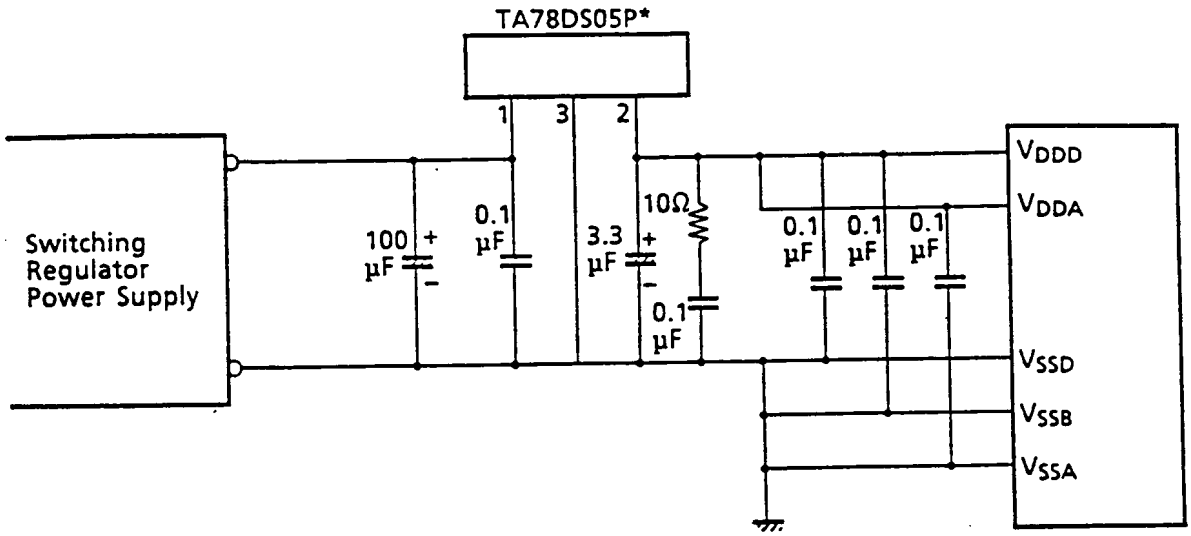


Fig. 8.5 Recommended Power Supply Circuit for TC8861F

* TA78DS05P has an input and output voltage difference of 0.3V (Maximum). Therefore it is suitable as a supply power in the recommended supply voltage range of 4.5-5.5V for TC8861F when the +5V switching regulator is used. In this case, it is enough if the switching regulator output is above 4.8V. However, output of 5.3V or above is desirable so as to get a central value (5.0V) of the recommended supply voltage range of TC8861F.

8.1.8 TC8861F List of Pins

Table 8.2 List of Pins on TC8861F

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
D0	4	I/O, 3-State	System controller data bus	*Hz
D1	3	I/O, 3-State	System controller data bus	*Hz
D2	2	I/O, 3-State	System controller data bus	*Hz
D3	1	I/O, 3-State	System controller data bus	*Hz
D4	59	I/O, 3-State	System controller data bus	*Hz
D5	58	I/O, 3-State	System controller data bus	*Hz
D6	57	I/O, 3-State	System controller data bus	*Hz
D7	56	I/O, 3-State	System controller data bus	*Hz
$\overline{\text{CHSET}}$	11	Input	Control signal from TC8862F	-
$\overline{\text{ADOUT}}$	9	Input	Control signal from TC8862F	-
$\overline{\text{STAR}}$	10	Input	Control signal from TC8862F	-
CK	7	Input	Clock input	-
$\overline{\text{RESET}}$	5	Input	Reset input	-
$\overline{\text{STBY}}$	8	Input	Stand-by input	-
$\overline{\text{ADRDY}}$	55	Output	TC8861F A to D operational status	H
MIN	36	Input	Microphone input	-
LIN	39	Input	Line input	-
CHML	40	Input	Analog input change-over signal	-
MOUT	41	Output	Output of MIC Amplifier or LIN Amplifier	Hz
PRIN	42	Input	Preamplifier input	-
POUT	43	Output	Preamplifier output	Hz
BPIN	44	Input	Band-pass filter input	-
VAN	37	Output	Grand level of analog signal on analog circuit (except MIN amplifier)	L
VANM	35	Output	Ground level of analog signal on MIN amplifier	L
VREFOUT	46	Output	Reference voltage for A to D circuit	4.0V**
BPF01	20	Output	Band-pass filter 1 output	Hz
RECI1	21	Input	Rectifier 1 input	-
BPF02	22	Output	Band-pass filter 2 output	Hz
RECI2	24	Input	Rectifier 2 input	-
BPF03	25	Output	Band-pass filter 3 output	Hz
RECI3	26	Input	Rectifier 3 input	-
BPF04	27	Output	Band-pass filter 4 output	Hz
RECI4	28	Input	Rectifier 4 input	-
BPF05	29	Output	Band-pass filter 5 output	Hz
RECI5	30	Input	Rectifier 5 input	-
BPF06	31	Output	Band-pass filter 6 output	Hz
RECI6	32	Input	Rectifier 6 input	-
BPF07	33	Output	Band-pass filter 7 input	Hz

* HZ=High impedance

** In case of V_{DD}=5.0V

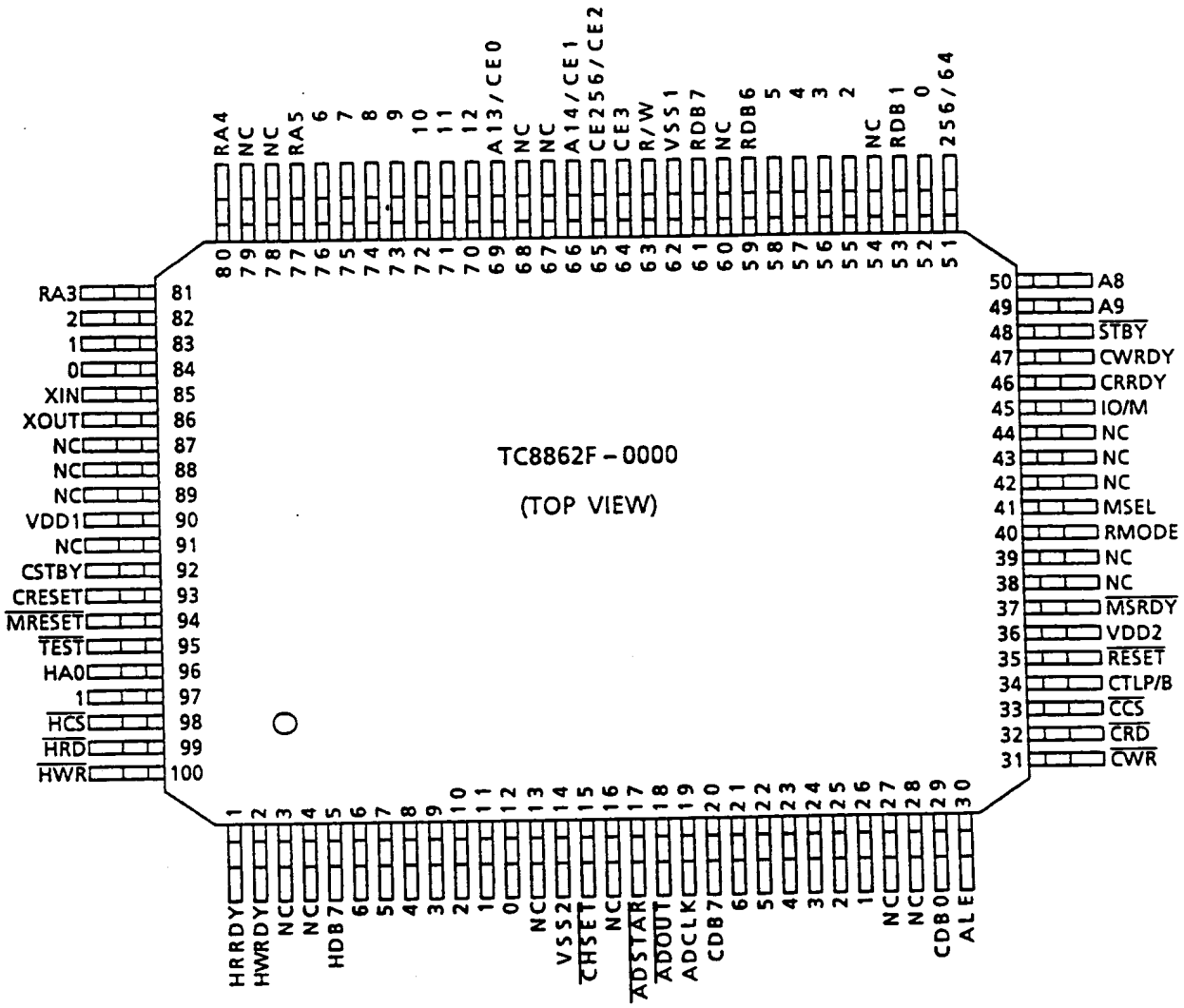
(Continued)

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
RECI7	34	Input	Rectifier 7 input	-
TIO0	19	Input/Output	Test Terminal	Hz
TIO2	18	Input/Output	Test Terminal	Hz
TIO3	17	Input/Output	Test Terminal	Hz
TVIN	45	Input	Test Terminal	-
$\overline{\text{SYNC}}$	16	Input	Test terminal: with a built-in pull-up resistor	-
$\overline{\text{TRESET}}$	15	Input	Test terminal: with a built-in pull-down resistor	-
$\overline{\text{TCHSET}}$	14	Input	Test terminal: with a built-in pull-up resistor	-
TDCEN	13	Input	Test terminal: with a built-in pull-down resistor	-
DTEST/ TDCSET	12	Input	Test terminal: with a built-in pull-down resistor	-
TADO	48	Input	Test terminal: with a built-in pull-down resistor	-
TΦ50	54	Output	Test terminal	L
TCOMP	47	Output	Test terminal	L
SHCK0	52	Output	Test terminal	L
SHCK1	51	Output	Test terminal	L
SHCK2	50	Output	Test terminal	L
SHCK3	49	Output	Test terminal	L
VDDD	53	–	Digital circuit power supply terminal	-
VDDA	23	–	Analog circuit ground supply terminal	-
VSSD	6	–	Digital circuit ground terminal	-
VSSB	60	–	Data bus buffer ground terminal	-
VSSA	38	–	Analog circuit ground terminal	-

8.2 TC8862F

8.2.1 TC8862F Pin Assignments

FP100 pin



NC: No Connection
Don't connect NC pins to any signal.

Fig. 8.6 TC8862F Pin Assignment Diagram

8.2.2 TC8862F Signal Descriptions

Controller I/F Signals

(1) CDB0~CDB7 (Controller Data Bus) [Input/Output]
8-bit bidirectional data bus connected to the internal bus in the recognition system for address and data input/output with TMP80C50AU. These terminals are to be connected to DB0-DB7 of TMP80C50AU.

(2) IO/M (I/O Memory select) [Input]
When H level signal is input to this terminal, I/O function in TC8862F is selected and when L level signal is input, Memory function is selected. The status of this terminal is latched at ALE falling edge. This terminal is to be connected to the P24 terminal of TMP80C50AU.

(3) MSEL (Memory SELect) [Input]
When H level signal is input to this terminal at IO/M=L as mentioned above, the reference pattern memory of TC8862F is selected. When L level signal is input, the scratch-pad RAM in TC8862F is selected. This terminal is also latched at ALE falling edge likewise the above-mentioned IO/M terminal. This terminal is to be connected to the P25 terminal of TMP80C50AU.

(4) RMODE (Reference memory access MODE) [Input]
When H level signal is input at IO/M=L and MSEL=H as mentioned above, the built-in reference pattern ROM is selected. When L level signal is input, the external reference pattern memory is selected. This terminal is also latched at ALE falling edge likewise the above-mentioned IO/M terminal.

(5) CTLP/B (ConTroL data Port/Bus select) [Input]
Normally, this terminal should be connected to VDD.

(6) ALE (Address Latch Enable) [Input]
At the falling edge of this terminal, addresses which are input through CDB0-CDB7 terminals and signals which are input through IO/M, MSEL and RMODE terminals are latched in TC8862F. This terminal is to be connected to the ALE terminal of TMP80C50AU.

(7) $\overline{\text{CRD}}$ (Controller ReaD strobe) [Input]
When L level signal is input to this terminal at $\overline{\text{CCS}}$=L as described later, CDB0-CDB7 terminals are put in the output mode. This terminal is to be connected to the $\overline{\text{RD}}$ terminal of TMP80C50AU.

(8) $\overline{\text{CWR}}$ (Controller WRite strobe) [Input]
At the rising edge of this terminal when $\overline{\text{CCS}}$=L as described later, CDB0-CDB7 data are latched in TC8862F. This terminal is to be connected to the $\overline{\text{WR}}$ terminal of TMP80C50AU.

(9) $\overline{\text{CCS}}$ (Controller Chip Select) [Input]
A low on this pin enables the TC8862F controller I/F to be active and the above-mentioned $\overline{\text{CRD}}$ and $\overline{\text{CWR}}$ terminals become valid. This terminal is usually to be connected to VSS.

(10) CRRDY (Controller Read ReaDY) [Output]
Read request signal output-terminal. To be connected to the P11 terminal of TMP80C50AU.

(11) CWRDY (Controller Write ReaDY) [Output]
Write enable signal output-terminal. To be connected to the P10 terminal of TMP80C50AU.

(12) A8, A9 (Address 8, 9) [Input]
Inner scratch pad RAM upper 2bit address input terminals. To be connected to the P20 and P21 terminals of TMP80C50AU.

(13) $\overline{\text{MSRDY}}$ (MS ReaDY) [Output]
Recognition calculation end signal output-terminal. When the recognition calculation for one word ends, this terminal becomes L level and when TMP80C50AU reads the result, it becomes H level. This terminal is to be connected to the T1 terminal of TMP80C50AU.

(14) $\overline{\text{RESET}}$ (System RESET) [Output]
System reset signal output-terminal. This terminal is to be connected to the $\overline{\text{RESET}}$ terminals of TC8861F and TMP80C50AU.

(15) $\overline{\text{STBY}}$ (STand-BY) [Output]
System stand-by signal output-terminal. To be connected to the $\overline{\text{STBY}}$ terminal of TC8861F and the $\overline{\text{PS}}$ terminal of TMP80C50AU.

TC8861F I/F Signals

(16) ADCLK (A to D CLocK) [Output]
TC8861F clock output-terminal. 2MHz, duty 50% signal is output. This terminal is to be connected to the CK terminal of TC8861F.

(17) $\overline{\text{CHSET}}$ (CHannel SET strobe) [Output]
TC8861F channel set signal output-terminal. This terminal is to be connected to the $\overline{\text{CHSET}}$ terminal of TC8861F.

(18) $\overline{\text{ADOUT}}$ (A to D read OUT strobe) [Output]
TC8861F A to D output data read-out signal output-terminal. This terminal is to be connected to the $\overline{\text{ADOUT}}$ terminal of TC8861F.

(19) $\overline{\text{ADSTAR}}$ (A to D STARt signal) [Output]
TC8861F A to D conversion start signal output-terminal. To be connected to the $\overline{\text{STAR}}$ terminal of TC8861F.

Host System I/F Signals

(20) HDB0~HDB7 (Host Data Bus) [Input/Output]
8-bit bidirectional data bus. These terminals are to be connected to the data bus of a host system and used for transferring all kinds of data such as commands, status and recognition result.

(21) HA0~HA1 (Host Port Address 0, 1) [Input]
These terminals are to be connected to the address output of a host system and used to specify the kind of data transferred through HDB0~7.

(22) $\overline{\text{HCS}}$ (Host Chip Select) [Input]
A low on this pin enables the TC8862F host system I/F to be active and the $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ terminals described below become valid.

(23) $\overline{\text{HRD}}$ (Host ReaD strobe) [Input]
When L level signal is input to this terminal at $\overline{\text{HCS}}$=L, the HDB0-HDB7 terminals are set to the output mode, and recognition result, status, etc. are output according to the signals of the HA0 and HA1 terminals. The $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ terminals must not be put at L level at the same time.

(24) $\overline{\text{HWR}}$ (Host WRite strobe) [Input]
At the rising edge of this terminal at $\overline{\text{HCS}}$=L as described above, HDB0-HDB7 data are latched in TC8862F. The $\overline{\text{HRD}}$ and $\overline{\text{HWR}}$ terminals should not be put at L level at one time.

(25) HRRDY (Host Read ReaDY) [Output]
Read request signal output-terminal. This terminal becomes H level when recognition result is set in the internal latch of TC8862F and becomes L level when a host system reads out the recognition result. Similar signal will be read out of the HDB0-HDB7 terminals as the status.

(26) HWRDY (Host WRite ReaDY) [Output]
Write enable signal output-terminal. When commands or data are acceptable to the recognition system, H level signal is output from this terminals. Likewise the HRRDY terminal, this signal also can be red out of the HDB0-HDB7 terminals.

Signals to Reset & Stand-by Circuits, Clock Oscillator

(27) CSTBY (Capacitor for STand-BY) [Input]
This terminal is connected with a capacitor and produces the system start sequence control timing when the power supply becomes ON.

(28) $\overline{\text{MRESET}}$ (Manual RESET) [Input]
Manual reset terminal with a built-in pull-up resistor. When L level signal is input to this terminal, the system can be reset. Since the reset operation is controllable by a host system, this terminal may be fixed at H level.

(29) CRESET (Capacitor for RESET) [Input/Output]
This terminal is used to produce the return timing from the reset and stand-by state by connecting a capacitor.

(30) XIN, XOUT (Xtal-IN, OUT) [Input, Output]
Ceramic resonator connecting terminals. A 4MHz ceramic resonator and capacitor are connected.

(31) $\overline{\text{TEST}}$ [Input]
Test input terminal with a built-in pull-up resistor. This terminal should be set at H level in normal operation.

External Reference Patterns memory I/F Signals

(32) RDB0~RDB7 (Reference memory Data Bus) [Input/Output]
8-bit bidirectional external reference pattern memory data bus. These terminals are to be connected to the external memory data bus. A pull-down resistor is connected to each of RDB0-RDB7 in LSI. These pull-down resistor will be cut off only when an external memory is accessed.

(33) RA0~RA12 (Reference memory Address) [Output]
The 13-bit external reference pattern memory address bus. These terminals are to be connected to the external memory address bus.

(34) A13/CE0, A14/CE1 [Output]
These terminals become the address output terminals when 256/64=H and the chip select output terminals when 256/64=L. These terminals are to be connected to the external reference pattern memory addresses A13 and A14 when 256/64=H and to the first and second 64Kbit memory chip select input terminals when 256/64=L.

(35) CE256/CE2 [Output]
This terminal becomes the 256Kbit memory chip select output terminal when 256/64=H and the third 64Kbit memory chip select output terminal when 256/64=L.

(36) CE3 [Output]
This terminal becomes the fourth 64Kbit memory chip select output terminal when 256/64=L. At 256/64=H, signal output keeps H level.

(37) R/W (Read/Write) [Output]
This terminal is to be connected to the R/W terminal of RAM when it is used as the external reference pattern memory. Nothing should be connected to this terminal when a ROM is used as the external reference memory.

(38) 256/64 (256K/64K memory select) [Input]
This terminal must be set at L level when the external reference pattern memory has a capacity of 64kbits and H level when it is 256Kbits.

Power Supply Signals

(39) VDD1, VDD2
The power supply terminals. Both terminals are to be connected to the plus side of the power supply.

(40) VSS1, VSS2
The ground terminals. Both terminals are to be connected to the ground side of the power supply.

8.2.3 TC8862F List of Pins

Table 8.3 List of Pins on TC8862F

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
CDB0	29	I/O	Controller data bus	*Hz
1	26	I/O	Controller data bus	*Hz
2	25	I/O	Controller data bus	*Hz
3	24	I/O	Controller data bus	*Hz
4	23	I/O	Controller data bus	*Hz
5	22	I/O	Controller data bus	*Hz
6	21	I/O	Controller data bus	*Hz
7	20	I/O	Controller data bus	*Hz
IO/M	45	Input	Control signal from TMP80C50AU	-
MSEL	41	Input	Control signal from TMP80C50AU	-
RMODE	40	Input	Control signal from TMP80C50AU	-
CTLP/B	34	Input	Control signal from TMP80C50AU	-
ALE	30	Input	Control signal from TMP80C50AU	-
$\overline{CRD}$	32	Input	Control signal from TMP80C50AU	-
$\overline{CWR}$	31	Input	Control signal from TMP80C50AU	-
$\overline{CCS}$	33	Input	Control signal from TMP80C50AU	-
CRRDY	46	Output	Status output for handshake operation	L
CWRDY	47	Output	Status output for handshake operation	H
A8	50	Input	Address signal from TMP80C50AU	-
A9	49	Input	Address signal from TMP80C50AU	-
$\overline{MSRDY}$	37	Output	Status output to TMP80C50AU	H
$\overline{RESET}$	35	Output	System reset output	L
$\overline{STBY}$	48	Output	System stand-by output	L
ADCLK	19	Output	TC8861F clock output	H
$\overline{CHSET}$	15	Output	TC8861F control signal	H
$\overline{ADOUT}$	18	Output	TC8861F control signal	H
$\overline{ADSTAR}$	17	Output	TC8861F control signal	H
HDB0	12	I/O	Host system data bus	Hz
1	11	I/O	Host system data bus	Hz
2	10	I/O	Host system data bus	Hz
3	9	I/O	Host system data bus	Hz
4	8	I/O	Host system data bus	Hz
5	7	I/O	Host system data bus	Hz
6	6	I/O	Host system data bus	Hz
7	5	I/O	Host system data bus	Hz
HA0	96	Input	Host system address bus	-
1	97	Input	Host system address bus	-
$\overline{HCS}$	98	Input	Control signal input from Host System	-
$\overline{HRD}$	99	Input	Control signal input from Host System	-

* Hz = High impedance

(Continued)

Pin Name	Pin No.	Input/Output	Function	Status at stand-by
$\overline{\text{HWR}}$	100	Input	Control signal input from Host System	-
HRRDY	1	Output	Status output to Host system for Handshake operation	L
HWRDY	2	Output	Status output to Host system for Handshake operation	L
CSTBY	92	Input	For producing rising start up timing	-
$\overline{\text{MRESET}}$	94	Input	Manual system reset input	-
CRESET	93	I/O	For producing reset and stand-by timing	L
XIN	85	Input	Ceramic resonator connecting terminal	-
XOUT	86	Output	Ceramic resonator connecting terminal	H
$\overline{\text{TEST}}$	95	Input	Test terminal with a built-in pull-up resistor	-
RDB0	52	I/O	External reference pattern memory data bus A pull-down resistor is connected in LSI except accessing	L
1	53	I/O	A pull-down resistor is connected in LSI except accessing	L
2	55	I/O	A pull-down resistor is connected in LSI except accessing	L
3	56	I/O	A pull-down resistor is connected in LSI except accessing	L
4	57	I/O	A pull-down resistor is connected in LSI except accessing	L
5	58	I/O	A pull-down resistor is connected in LSI except accessing	L
6	59	I/O	A pull-down resistor is connected in LSI except accessing	L
7	61	I/O	A pull-down resistor is connected in LSI except accessing	L
RA0	84	Output	External reference pattern memory address bus	L
1	83	Output	External reference pattern memory address bus	L
2	82	Output	External reference pattern memory address bus	L
3	81	Output	External reference pattern memory address bus	L
4	80	Output	External reference pattern memory address bus	L
5	77	Output	External reference pattern memory address bus	L
6	76	Output	External reference pattern memory address bus	L
7	75	Output	External reference pattern memory address bus	L
8	74	Output	External reference pattern memory address bus	L
9	73	Output	External reference pattern memory address bus	L
10	72	Output	External reference pattern memory address bus	L
11	71	Output	External reference pattern memory address bus	L

(Continued)

Pin Name	Pin No.	Input/Output	Function	Status at standby
RA12	70	Output	External reference pattern memory address bus	L
A13/CE0	69	Output	External reference pattern memory address & chip selection	H
A14/CE1	66	Output	External reference pattern memory address & chip selection	H
CE256/CE2	65	Output	External reference pattern chip selection	H
CE3	64	Output	External reference pattern chip selection	H
R/W	63	Output	External reference pattern RAM read/write control signal	H
256/64	51	Input	External reference pattern memory type select	-
VDD1	90	-	Power supply terminal	-
VDD2	36	-	Power supply terminal	-
VSS1	62	-	Ground	-
VSS2	14	-	Ground	-

8.3 TMP80C50AU

8.3.1 TMP80C50AU Pin Assignments

μFP 44 pin

NC: No Connection
Don't connect NC pins
to any signal.

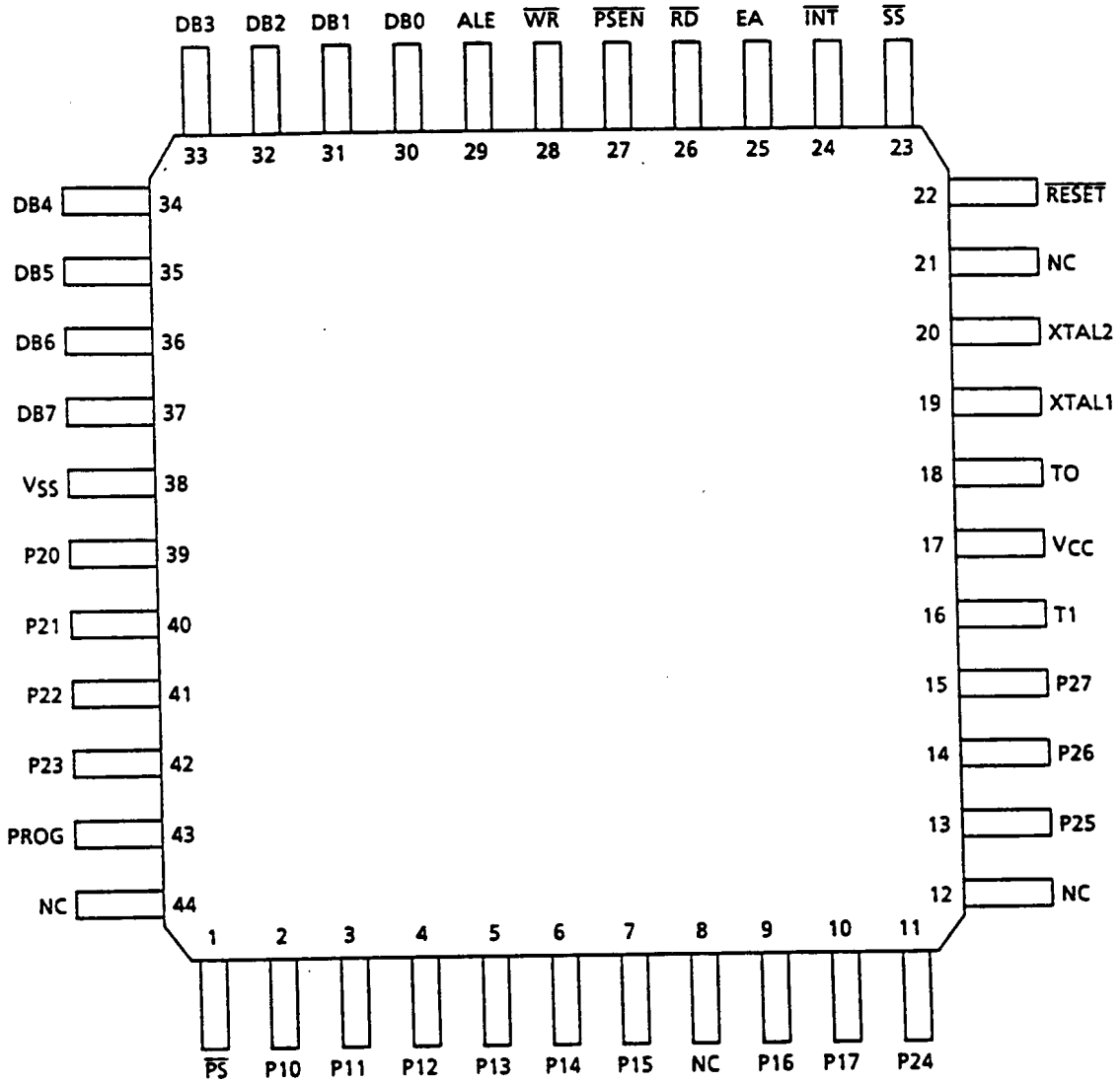


Fig. 8.7 TMP80C50AU Pin Assignment Diagram

8.3.2 TMP80C50AU Signal Description

(1) XTAL1, XTAL2 [Input]
Ceramic resonator connecting terminals. An 11MHz ceramic resonator and capacitors are to be connected to these terminals.

(2) $\overline{\text{RESET}}$ (system RESET) [Input]
Reset terminal. When this terminal is set at L level, TMP80C50AU is reset. When it is returned to H level again, it starts to operate. This terminal is to be connected to the $\overline{\text{RESET}}$ terminal of TC8862F.

(3) $\overline{\text{INT}}$ (INTerrupt) [Input]
TC8861F A to D conversion status signal input-terminal. To be connected to the $\overline{\text{ADRDY}}$ terminal of TC8861F.

(4) T1 [Input]
TC8862F multiple similarity calculation status signal input-terminal. To be connected to the $\overline{\text{MSRDY}}$ terminal of TC8862F.

(5) ALE (Address Latch Enable) [Output]
Address latch enable signal. It gives a timing signal to latch into TC8862F addresses, which are output to the CDB0-CDB7 terminal at the falling edge of this signal. To be connected to the ALE terminal of TC8862F.

(6) DB0~DB7 (Data Bus) [Input/Output]
8-bit bidirectional data bus. To be connected to the inner bus of the recognition system.

(7) $\overline{\text{RD}}$ (ReaD strobe) [Output]
This terminal is connected to the $\overline{\text{CRD}}$ terminal of TC8862F and used to read data from TC8862F through DB0~DB7.

(8) $\overline{\text{WR}}$ (WRite strobe) [Output]
This terminal is connected to the $\overline{\text{CWR}}$ terminal of TC8862F and used to write data to TC8862F through DB0~DB7.

(9) $\overline{\text{PS}}$ (Power Save) [Input]
Stand-by input terminal. To be connected to the $\overline{\text{STBY}}$ terminal of TC8862F. When L level signal is input to this terminal, TMP80C50AU is placed in the stand-by state. In this case, however, the RESET terminal must have been set at L level in advance.

(10) P10 (Port 10) [Input]
CWRDY signal input-terminal from TC8862F.

(11) P11 (Port 11) [Input]
CRRDY signal input terminal from TC8862F.

(12) P20, P21 (Port 20, 21) [Output]
Upper addresses of scratch-pad RAM of TC8862F. To be connected to the A8 and A9 terminals of TC8862F.

(13) P24 (Port 24) [Output]
Output terminal to the IO/M terminal of TC8862F.

(14) P25 (Port 25) [Output]
Output terminal to the MSEL terminal of TC8862F.

(15) P26 (Port 26) [Output]
This signal specifies how to use the reference pattern of TC8862F.

(16) VDD
Power supply terminal. To be connected to the plus side of power supply.

(17) VSS
Ground terminal. To be connected to the ground side of the power supply.

(18) EA [Input]
Input terminal. This terminal must be set at L level.

(19) $\overline{SS}$ [Input]
Input terminal. This terminal must be set at H level.

(20) $\overline{PSEN}$ [Output]
Output terminal. Nothing should be connected.

(21) T0 [Input]
Input terminal. This terminal should be set at L level.

(22) PROG [Output]
Output terminal. Nothing should be connected.

(23) P12~P17 (Port 12~17) [Input/Output]
Input/output terminal with built-in pull-up resistor. It becomes output on testing. Nothing should be connected.

(24) P22, P23 (Port 22, 23) [Input]
Input terminal with built-in pull-up resistor like P12~P17. Nothing should be connected.

(25) P27 (Port 27) [Input]
Input terminal. This terminal should be set at L level.

Note) Nothing should be connected to the NC terminal.

9. Electrical characteristics

9.1 TC8861F

9.1.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	−0.3~+6.0	V
Input Voltage	VIN	−0.3~VDD+0.3	V
Output Voltage	VOUT	−0.3~VDD+0.3	V
Storage Temperature	Tstg	−55~+125	°C

9.1.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	4.5~5.5	V
Input Voltage	VIN	0~VDD	V
Output Voltage	VOUT	0~VDD	V
Operating Frequency	fCLK	1.9~2.1	MHz
Operating Temperature	Topr	0~+70	°C

9.1.3 DC Characteristics (V_{DD} = +5.0V ± 10%, T_{opr} = 0~+70°C)

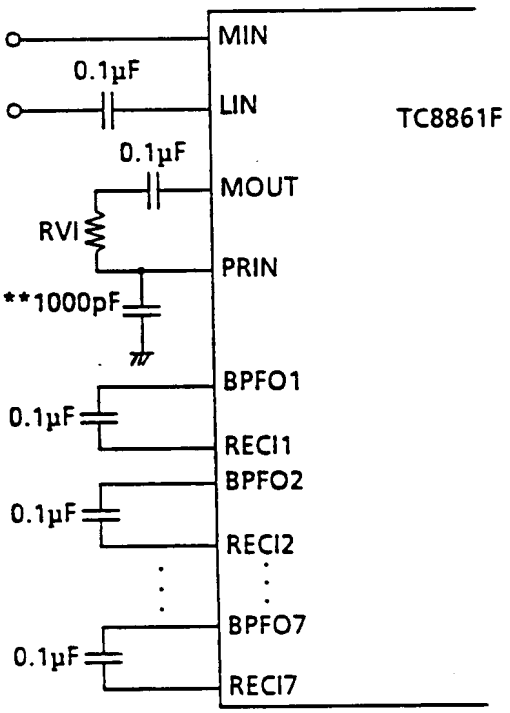
CHARACTERISTIC		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Input Low Voltage		VIL		−	−	0.8	V
Input High Voltage	D0~D7	VIH		2.2	−	−	V
	Other than above			VDD−0.8	−	−	
Input Low Current		IIL	VIN = 0V	−	−	−5	μA
Input High Current		IIH	VIN = VDD	−	−	−5	μA
Output Low Current		IOL	VOUT = 0.4V	1.76	−	−	mA
Output High Current		IOH	VOUT = VDD−0.4V	−0.44	−	−	

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
Supply Current (1)	IDD-OPR	When A to D Converter not operating	–	13	25	mA
Supply Current (2)	IDD-STBY	At stand-by state	–	–	3	μA

9.1.4 Analog Input Terminal (VDD = +5.0V ± 10%, T_{opr} = 0~ +70°C)

ITEM		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Allowable input	MIN	Vin	RVI* = 0KΩ f = 1KHz	–	–	28	mVp-p
	LIN		RVI* = 75KΩ f = 1KHz	–	–	250	
Input Resistance	MIN	Rin	f = 1KHz	–	100	–	KΩ
	LIN			–	100	–	

* Condition: The following parts wiring scheme is employed.



** 1000pF condenser is essential for normal operation

Fig. 9.1 Wiring Diagram

9.2 TC8862F

9.2.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	−0.3~+6.0	V
Input Voltage	VIN	−0.3~VDD+0.3	V
Output Voltage	VOUT	−0.3~VDD+0.3	V
Storage Temperature	Tstg	−55~+125	°C

9.2.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	4.5~5.5	V
Input Voltage	VIN	0~VDD	V
Output Voltage	VOUT	0~VDD	V
Operating Frequency	fCK	3.8~4.2	MHz
Operating Temperature	Topr	0~+70	°C

9.2.3 DC Characteristics

CHARACTERISTIC		SYMBOL	TEST CONDITION	RATING			UNIT
				MIN.	TYP.	MAX.	
Input Low Voltage		VIL		−	−	0.8	V
Input High Voltage	$\overline{\text{MRESET}}$ 256/64	VIH		VDD−0.8	−	−	V
	Other than above			2.2	−	−	
Input Low Current	$\overline{\text{MRESET}}$	IIL	VIN=0V	−	−11	−	μA
	Other than above			−	−	−5	
Input High Current	RDB0~7	IIH	VIN=VDD	−	+11	−	μA
	Other than above			−	−	5	
Output High Current		IOL	VOUT=0.4V	1.76	−	−	mA
Output High Current		IOH	VOUT=VDD−0.4V	−0.44	−	−	mA
Supply Current (1)		IDD-OPR	In no access state	−	1	5	mA
Supply Current (2)		IDD-STBY	In stand-by state	−	−	3	μA

9.2.4 AC Characteristics [VDD = +5.0V ± 10%, fCK = 4MHz, T_{opr} = 0~ +70°C, CL = 20PF (Control Signal). 100PF (Data Bus)]

(1) Host System I/F Reading Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{HRD}$ Pulse Width	tHRR		300	–	10000	ns
Address Setup Time	tHAR		0	–	–	ns
Output Delay Time	tHRD		–	–	200	ns
Address Hold Time	tHRA		0	–	–	ns
Output Disable Time	tHDF		10	–	100	ns

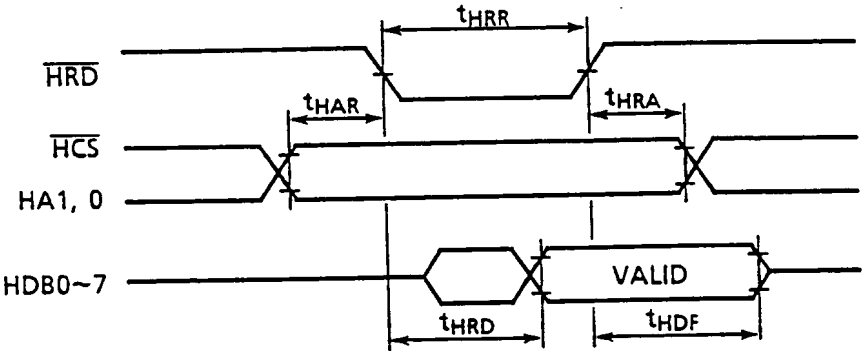


Fig. 9.2 Reading Cycle Timing Diagram on TC8862F Host Interface

(2) Host System I/F Writing Cycle

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
$\overline{HWR}$ Pulse Width	tHWW		300	–	10000	ns
Address Setup Time	tHAW		0	–	–	ns
Data Setup Time	tHDW		120	–	–	ns
Address Hold Time	tHWA		0	–	–	ns
Output Disable Time	tHWD		30	–	–	ns

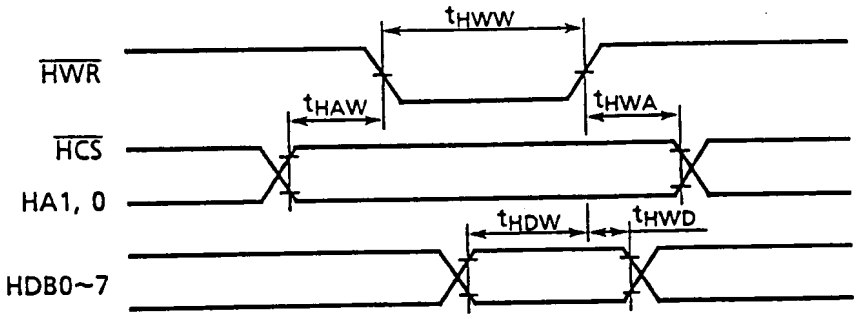


Fig. 9.3 Writing Cycle Timing Diagram on TC8862F Host Interface

(3) External Reference Pattern Memory I/F Reading Cycle with 64K Memory

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
CE Pulse Width	tRRR	256/64 = L,FCK = 4MHz	1.45	–	1.55	μs
Address Setup Time	tRAR	256/64 = L,FCK = 4MHz	2.45	–	–	μs
Address Hold Time	tRRA	256/64 = L,FCK = 4MHz	0	–	–	μs
Data Setup Time	tRRS	256/64 = L,FCK = 4MHz	1	–	–	μs
Data Hold Time	tRRH	256/64 = L,FCK = 4MHz	0	–	1	μs

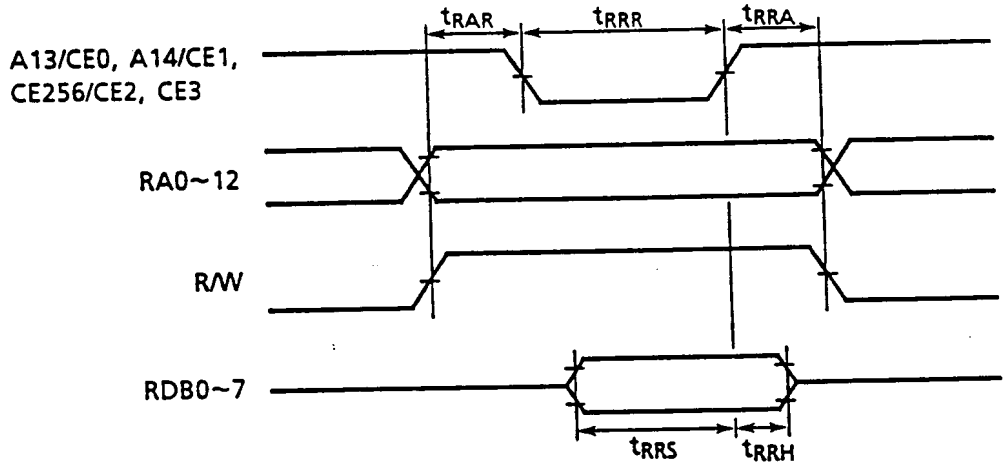


Fig. 9.4 Reading Cycle Timing Diagram on TC8862F External Reference Pattern Memory Interface with 64K Memory

(4) External Reference Pattern Memory I/F Writing Cycle with 64K RAM

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
CE Pulse Width	tRWW	256/64 = L,FCK = 4MHz	700	–	800	ns
Address Setup Time	tRAW	256/64 = L,FCK = 4MHz	250	–	–	ns
Address Hold Time	tRWA	256/64 = L,FCK = 4MHz	500	–	–	ns
Data Setup Time	tRDW	256/64 = L,FCK = 4MHz	1200	–	–	ns
Data Hold Time	tRWD	256/64 = L,FCK = 4MHz	100	–	–	ns

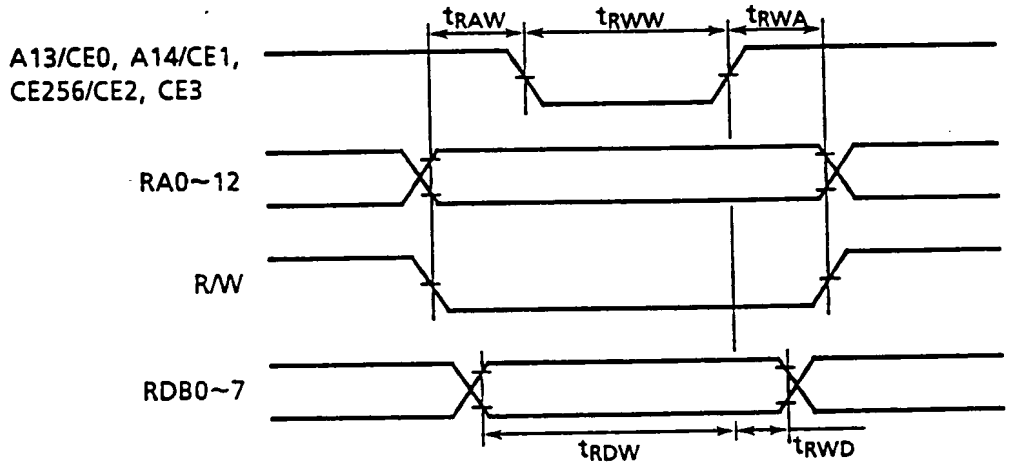


Fig. 9.5 Writing Cycle Timing Diagram on TC8862F External Reference pattern Memory Interface with 64K RAM

(5) External Reference Pattern Memory I/F Reading Cycle with 256Kbit Memory

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
CE Pulse Width	tRRR	256/64 = H,FCK = 4MHz	1.45	–	1.55	μs
Address Setup Time	tRAR	256/64 = H,FCK = 4MHz	2.45	–	–	μs
Address Hold Time	tRRA	256/64 = H,FCK = 4MHz	0	–	–	μs
Data Setup Time	tRRS	256/64 = H,FCK = 4MHz	1	–	–	μs
Data Hold Time	tRRH	256/64 = H,FCK = 4MHz	0	–	1	μs

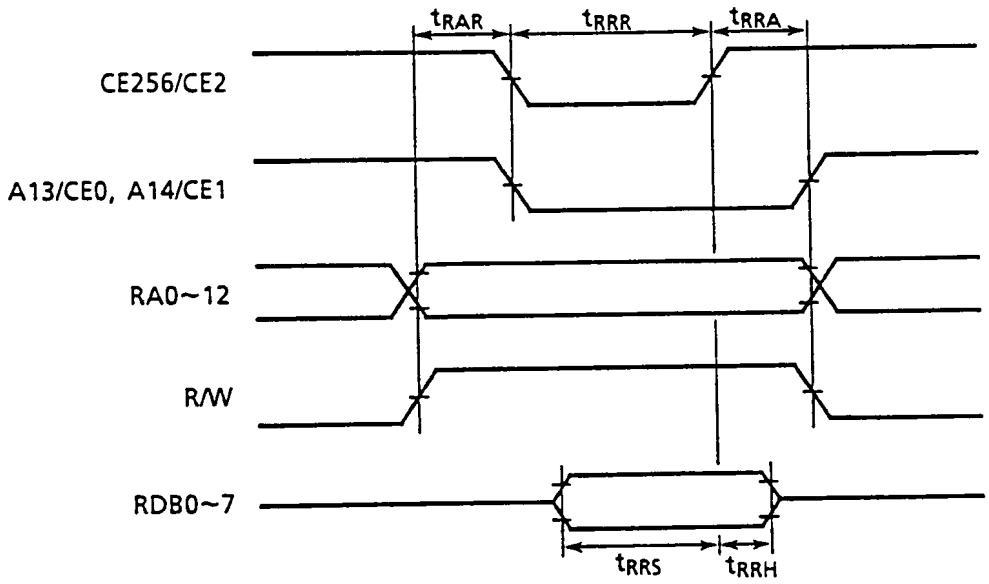


Fig. 9.6 Reading Cycle Timing Diagram on TC8862F External Reference Pattern Memory Interface with 256K Memory

(6) External Reference Pattern Memory I/F Writing Cycle with 256Kbit RAM

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
CE Pulse Width	tRWW	256/64 = H,FCK = 4MHz	700	–	800	ns
Address Setup Time	tRAW	256/64 = H,FCK = 4MHz	250	–	–	ns
Address Hold Time	tRWA	256/64 = H,FCK = 4MHz	500	–	–	ns
Data Setup Time	tRDW	256/64 = H,FCK = 4MHz	1200	–	–	ns
Data Hold Time	tRWD	256/64 = H,FCK = 4MHz	100	–	–	ns

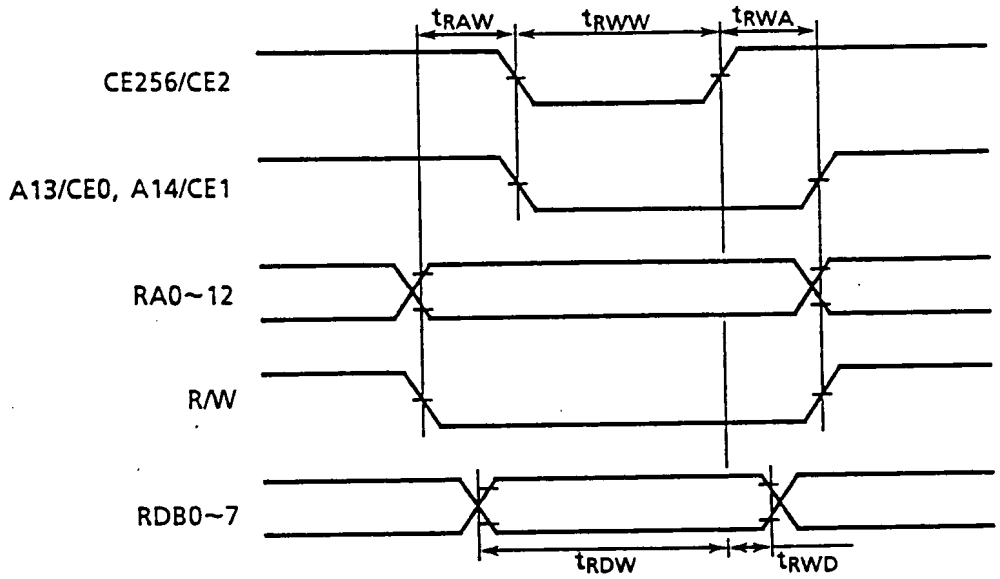


Fig. 9.7 Writing Cycle Timing Diagram on TC8862F External Reference Pattern Memory Interface with 256K RAM

9.3 TMP80C50AU

9.3.1 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	−0.3~+6.0	V
Input Voltage	VIN	−0.3~VDD+0.3	V
Output Voltage	VOUT	−0.3~VDD+0.3	V
Storage Temperature	TSTG	−55~+125	°C

9.3.2 Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	4.5~5.5	V
Input Voltage	VIN	0~VDD	V
Output Voltage	VOUT	0~VDD	V
Operating Frequency	fCK	10.45~11.55	MHz
Operating Temperature	Topr	0~+70	°C

9.3.3 DC Characteristics

TOPR = 0~ +70°C, VDD = +5.0V ± 10%, VSS = 0V

CHARACTERISTIC	SYMBOL	TEST CONDITION	RATING			UNIT
			MIN.	TYP.	MAX.	
Input Low Voltage	VIL		−0.5	−	0.8	V
Input High Voltage (XTAL1, XTAL2 Except $\overline{RESET}$, $\overline{STBY}$)	VIH		2.2	−	VDD	V
Input High Voltage (XTAL1, XTAL2 $\overline{RESET}$, $\overline{STBY}$)	VIH1		0.7×VDD	−	VDD	V
Supply Current	IDD-OPR	VDD = 5V, fCK = 11MHz Vin = 4.8V/0.2V	−	−	15.0	mA
Stand-by Current	IDD-STBY	VDD = 5V, VIH = VDD-0.2V VIL = 0.2V	−	0.5	10	μA

10. Package Dimensions

10.1 TC8861F

60-pin Mini-Flat Package

Unit : mm

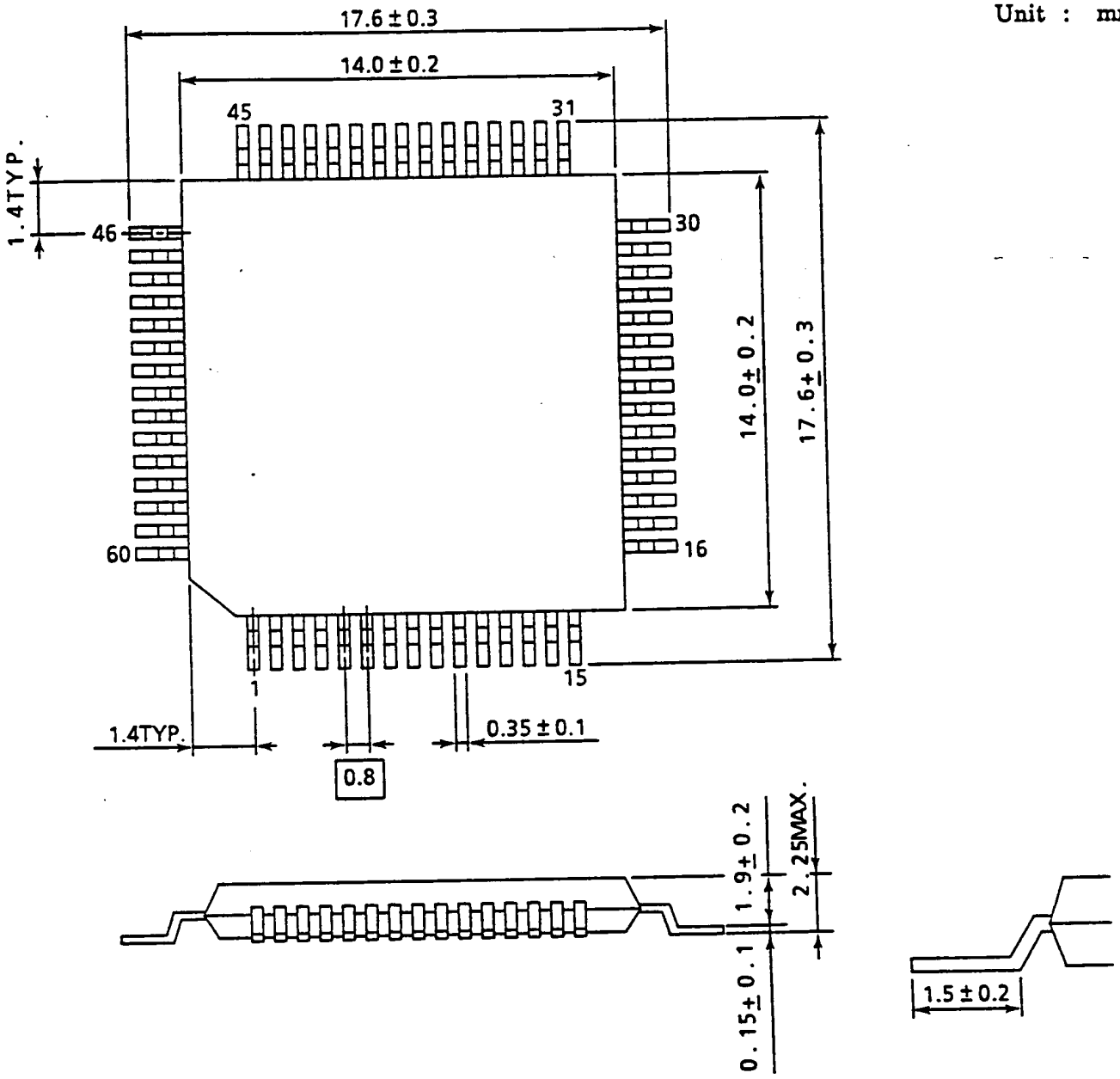


Fig 10.1 TC8861F Package Dimensions Diagram

10.2 TC8862F

100-pin Flat Package

Unit : mm

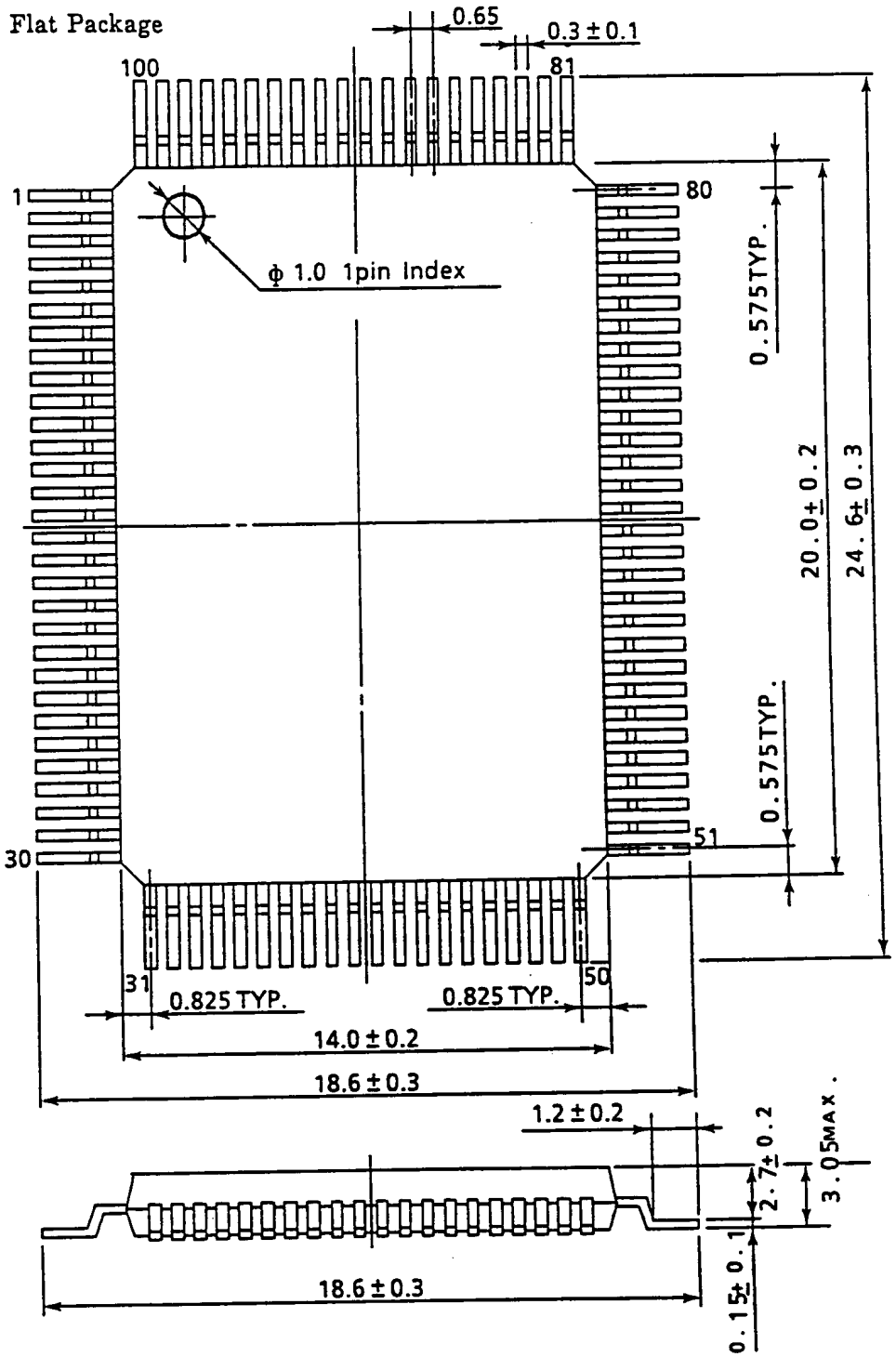
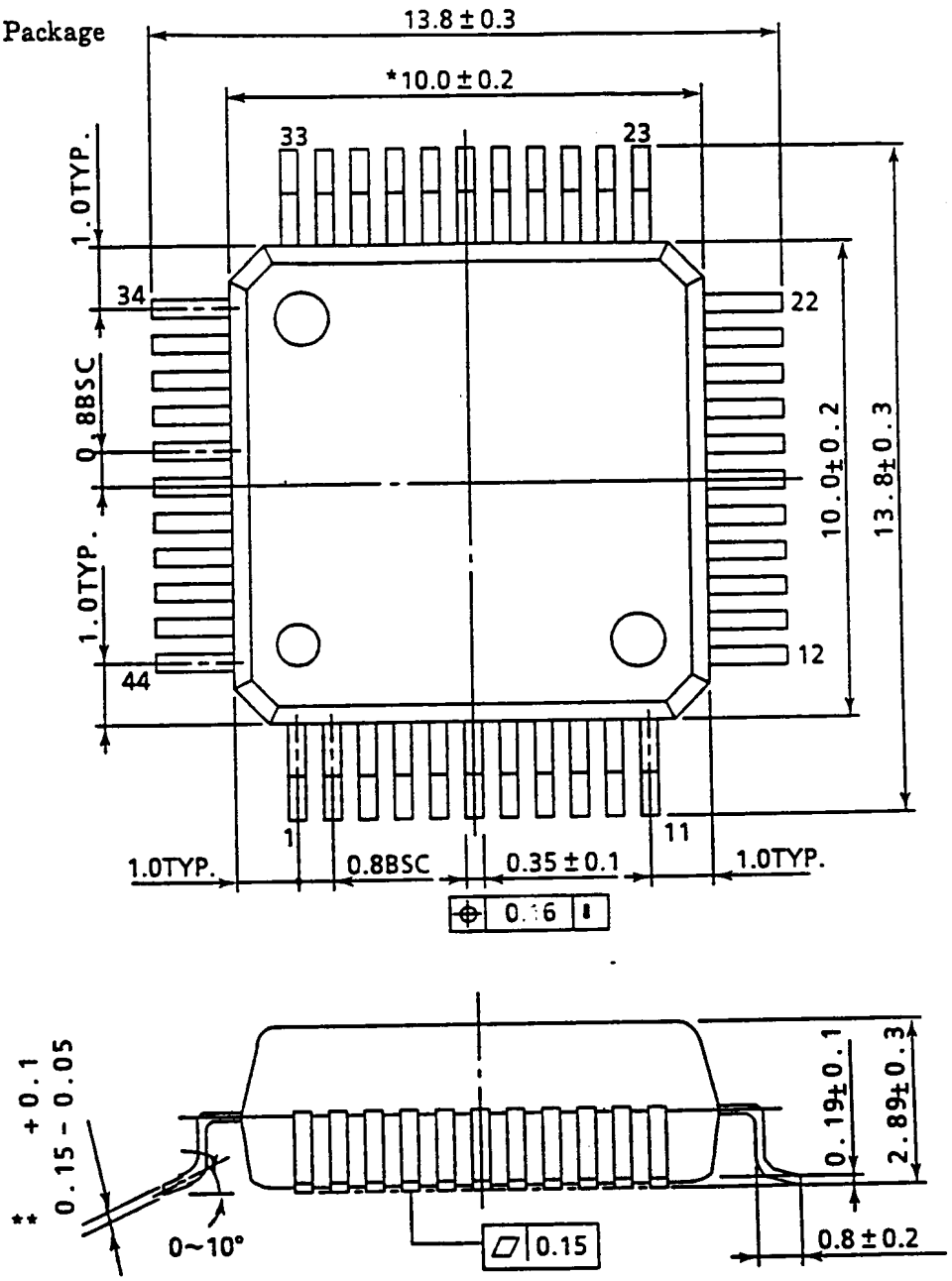


Fig. 10.2 TC8862F Package Dimensions Diagram

10.3 TMP80C50AU

44-pin Micro-Flat Package

Unit : mm



* Resin burr and residual tie bar cut are excluded.
Resin burr and residual tie bar cut shall be 0.15 maximum.

** Applied to the flat section of the lead.

Fig. 10.3 TMP80C50AU Package Dimensions Diagram